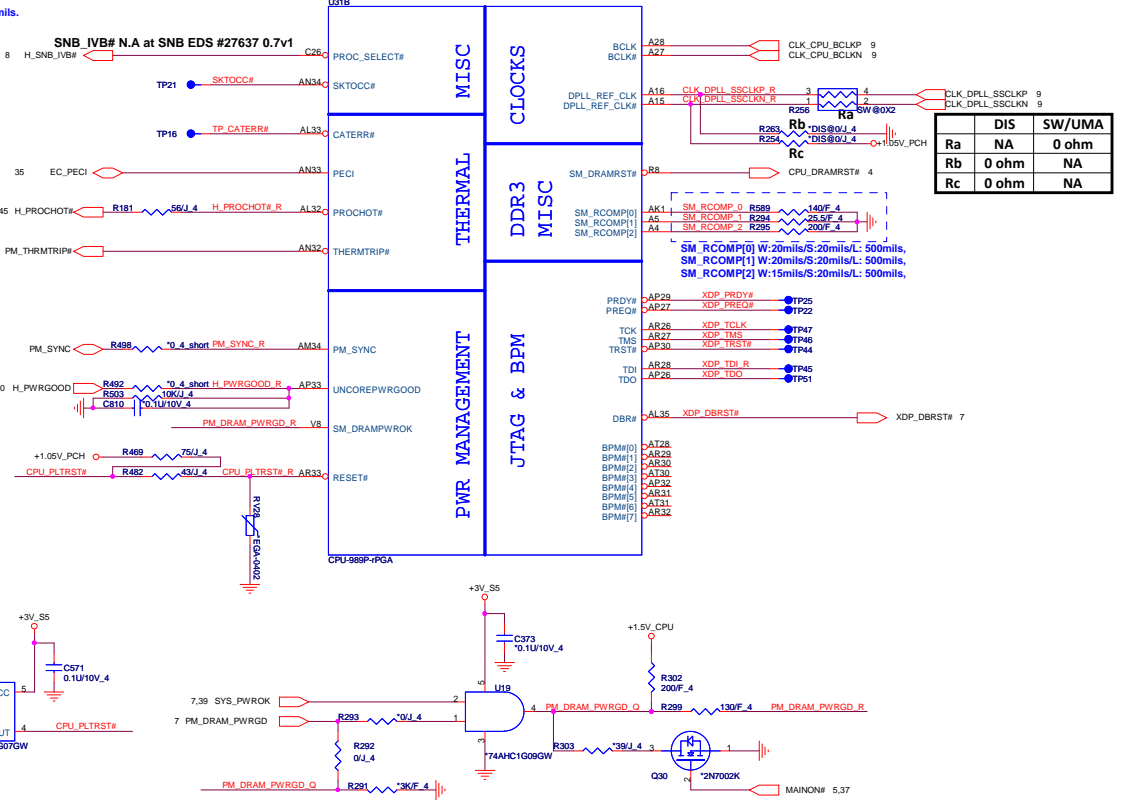


Table of Contents	
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	PineView CPU
8-13	TigerPoint
14	DDRII SO-DIMM
15	LCD Conn
16	CRT Conn.
17	Audio Codec CX20582
18	LAN(RTL8103EL/8111DL)
19	SATA HDD
20	USB x 3
21	CardReader AU6433
22	MINI-Card (WLAN)
23	MINI-Card (WWAN)
24	BLUETOOTH
25	KB/TP
26	SW/LED/Other
27	FAN & Thermal
28	KBC IT8502E
29	HOLD & SKEW
30	Discharge
31	Charger
32	DDR 1.8V (TPS51116)
33	VCCP (OZ8116LN)
34	3V/5V (ISL6237)
35	VCore (ISL6261A)
36	VCC1.5V/ GFX CORE
37	Power Block Dianram
38	
39	
40	

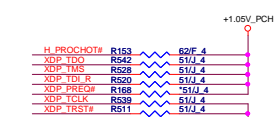
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,30,31,32,33,34,35	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	11,12,38	RTC		S0-S5
3VPCU	+3.3V	11,15,18,25,26,28,30,31,34,36	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	11,30,31,32,33,34,36	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	15,30,32,34	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	18,30	LAN POWER	LAN_ON	
5V_S5	+5V	12,20,30	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,11,12,21,22,30	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WIMAX POWER	S5_ON	S0-S3
5VSUS	+5V	15,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	26,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0-S3
+VCC_GFX_CORE	+0.9V~+1.2V	6,36	VGA CORE POWER	MAIN_ON	S0
0.9VSMDDR_VTERM	+0.75V	5,14,32	DDR2 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,15,16,17,19,25,27,28,30	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,6,9,10,11,12,14,15,16,17,18,19,21,22,23,24,26,28,30,32,33,34,35	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,21,32	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	6,8,12,17,22,23,36	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V	+1.05V	3,4,6,9,12,30,33	PCH CORE POWER	MAIN_ON	S0
VCC_CORE		6,30,35	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	L_VDD_EN	S0
BAT-V	+10V~+17V	31	MAIN BATTERY	CHG_PBATT	S0-S5

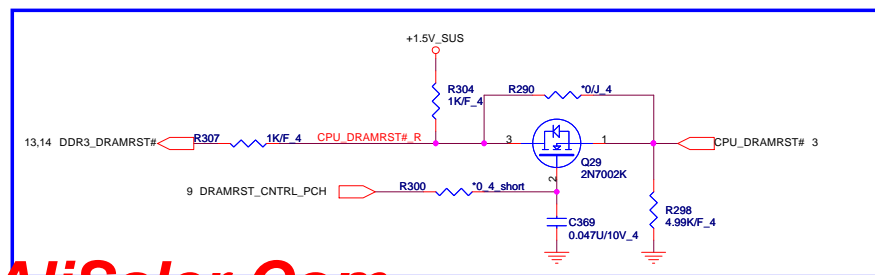
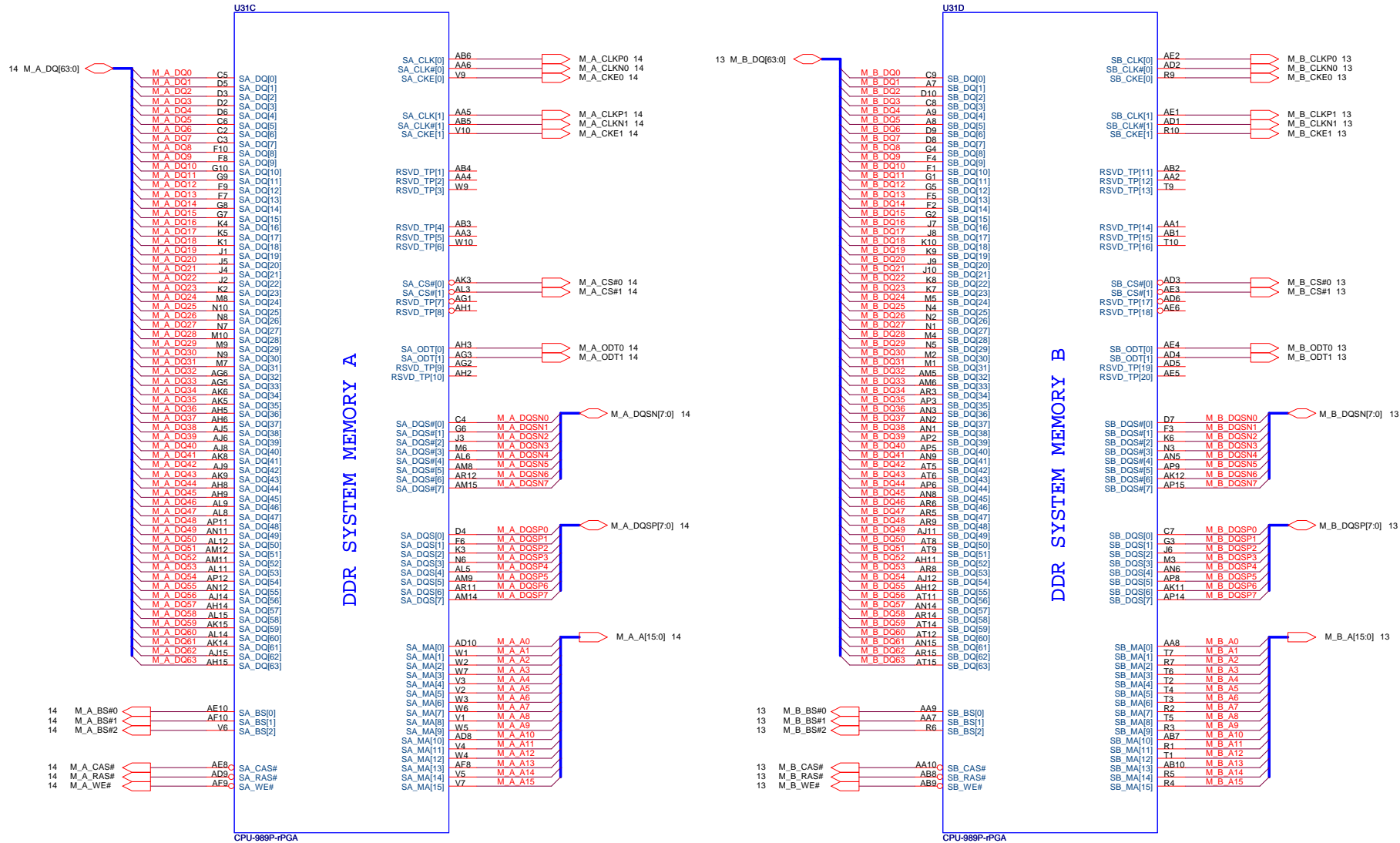
Sandy Bridge Processor (CLK,MISC,JTAG)



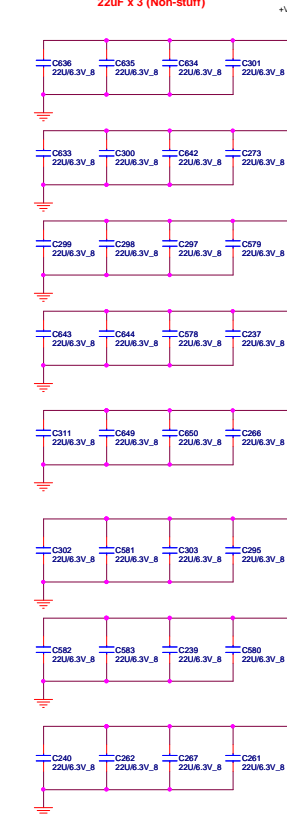
Processor pull-up(CPU)



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	Sandy Bridge 1/4	1A
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CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)



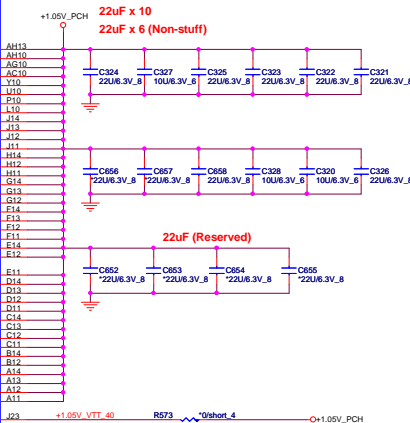
Reserved

C243
*22U/6.3V_8

C238
*22U/6.3V_8

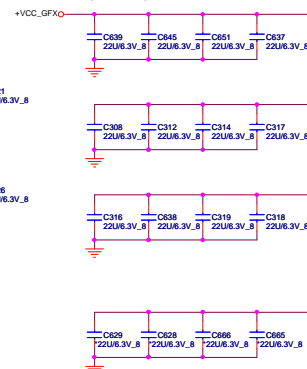
C263
*22U/6.3V_8

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-s

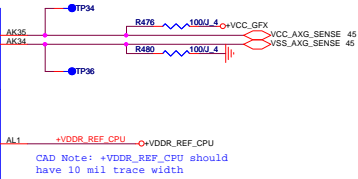
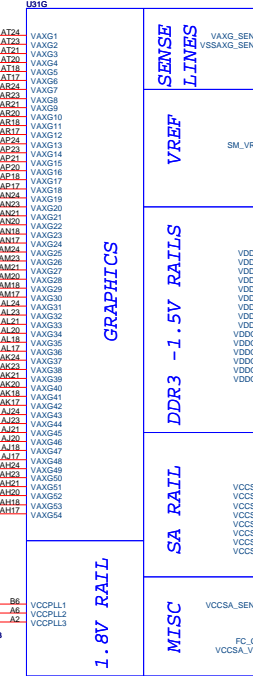


CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

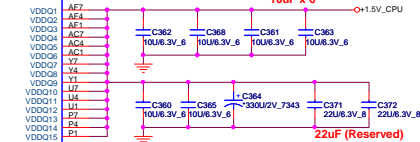
CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Rese



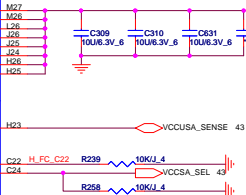
GRAPHICS



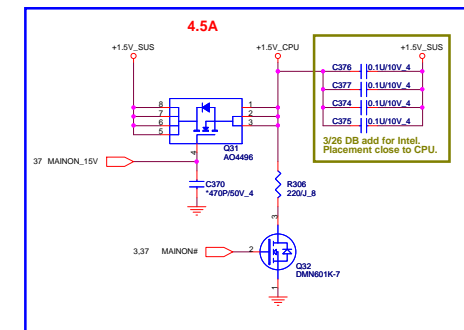
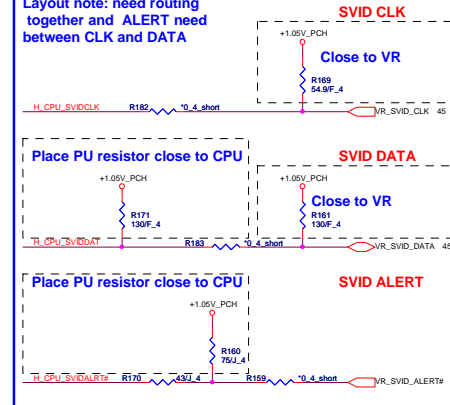
CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6



CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3



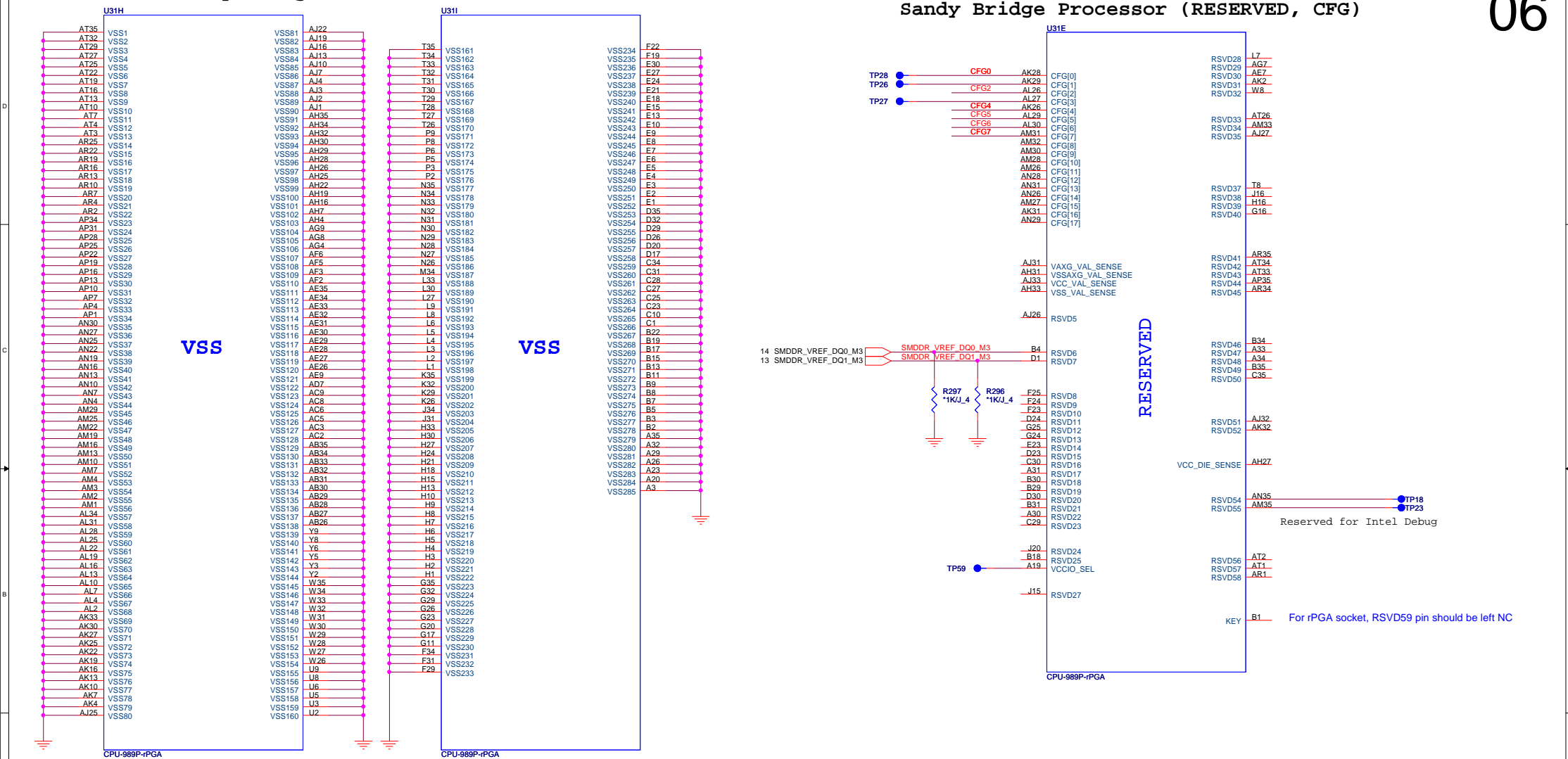
Layout note: need routing together and ALERT need between CLK and DATA



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

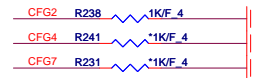
06



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



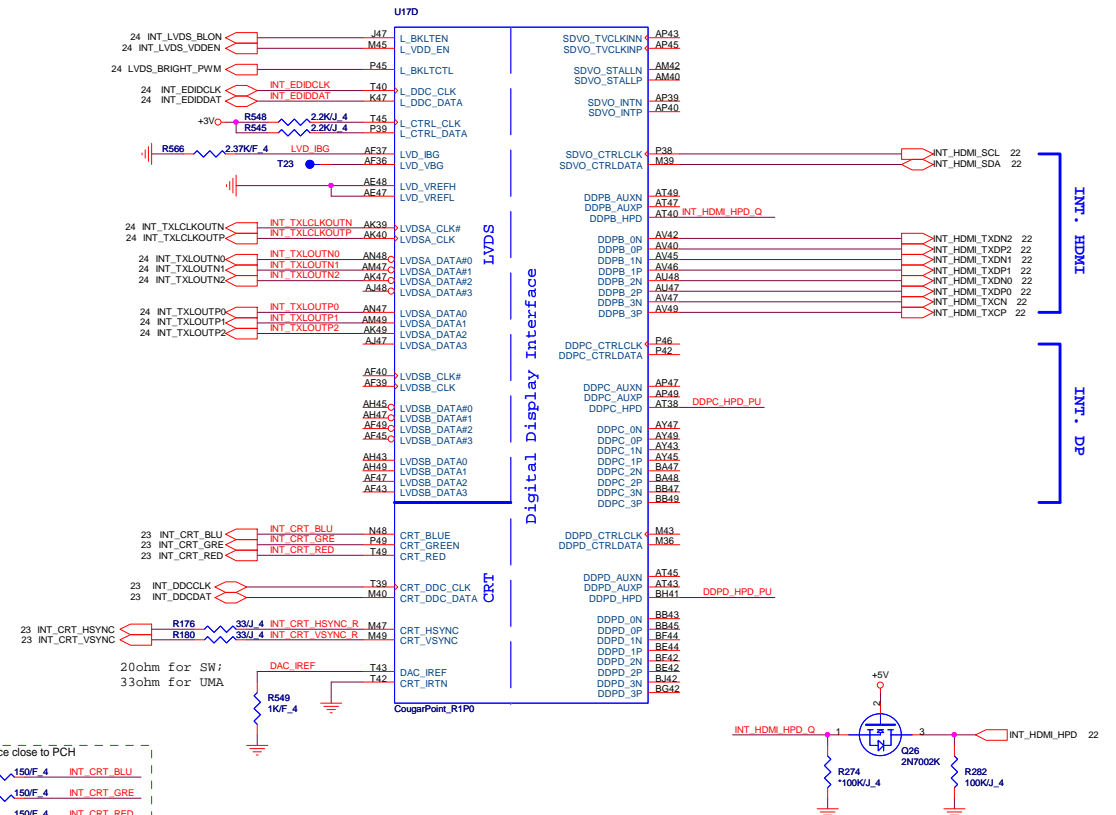
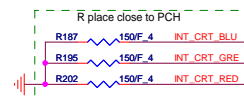
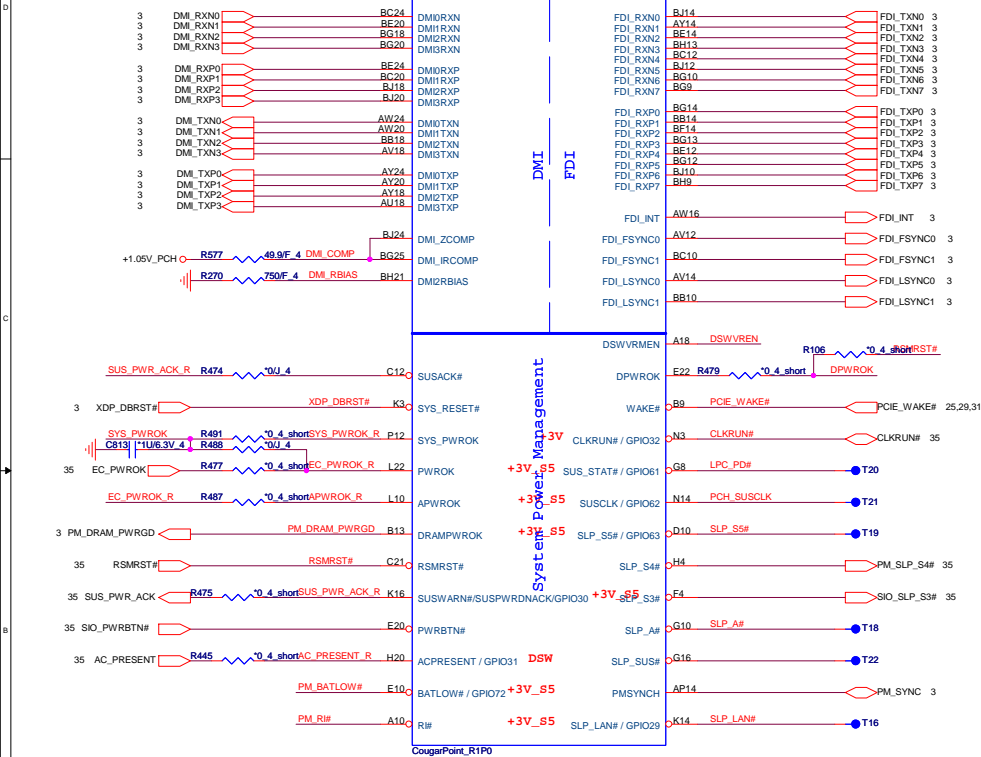
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

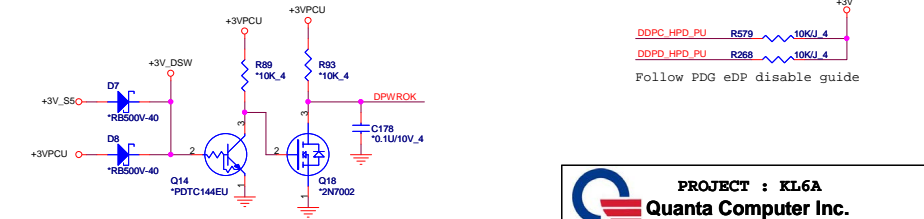
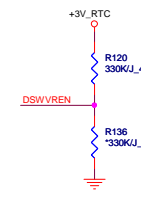
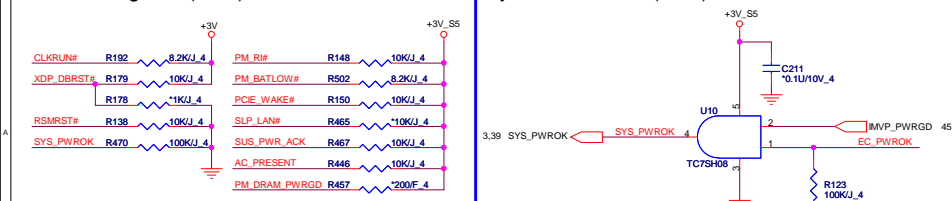
PROJECT : KL6A
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Sandy Bridge 4/4
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U17C



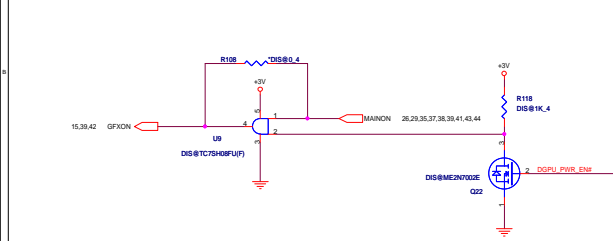
System PWR_OK(CLG)



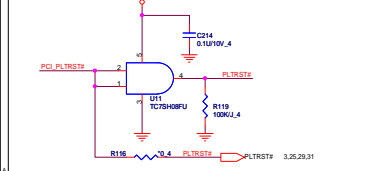
08

Cougar Point-M (PCI-E,SMBUS,CLK)

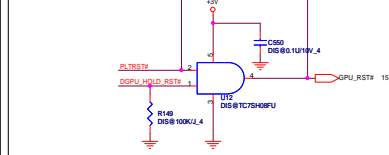
DGPU Power ON



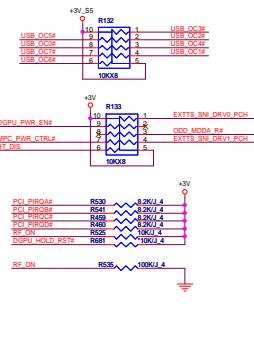
PLTRST#(CLG)



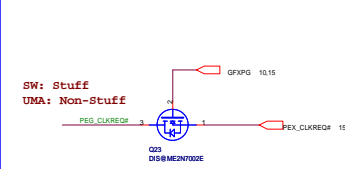
GPU RST#(CLG)



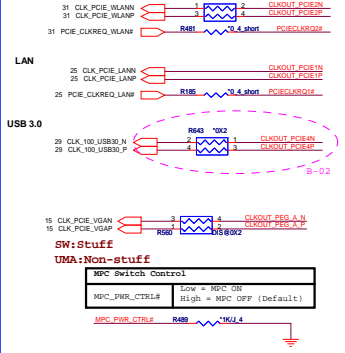
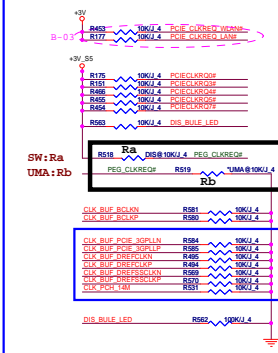
PCI/USBOC# Pull-up(CLG)



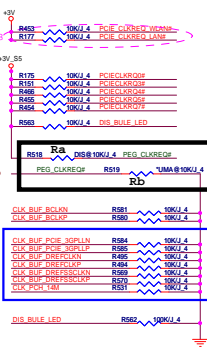
PEG CLK detect



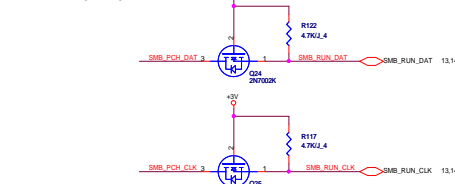
WLAN

[illegible]

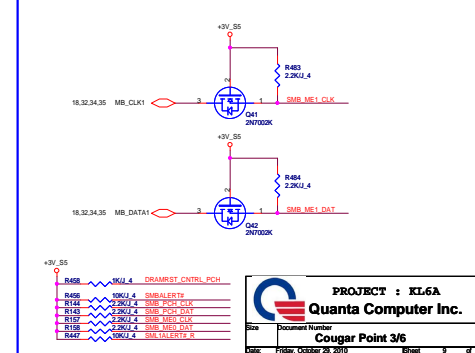
CLK_REQ/Strap Pin(CLG)



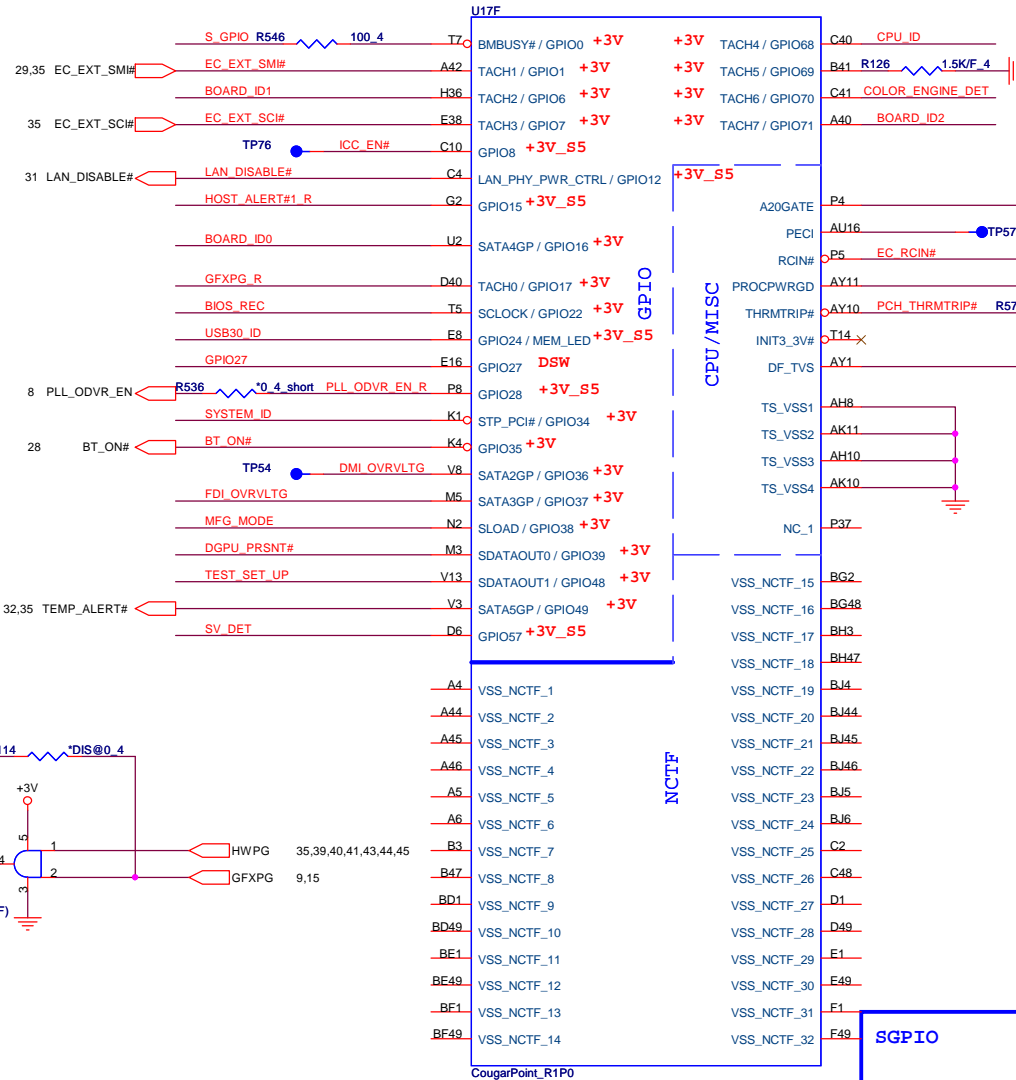
SMBus(CLK)



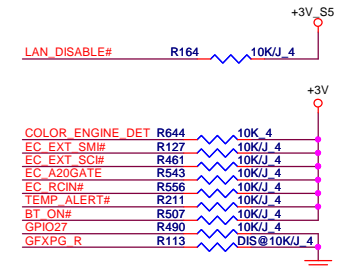
SMBus/Pull-up(CLG)



Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

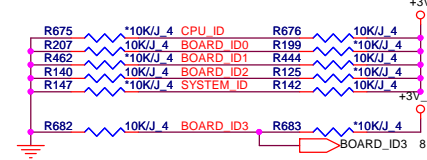


Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID3 GPIO13	ID1 GPIO6	ID0 GPIO16	CPU_ID GPIO68	Board ID
SDV	1	1	0	0	0	1	B-04
SIV	1	1	0	0	1	1	
SIT	1	1	0	1	0	1	
SVT	1	1	0	1	1	1	
SOVP	1	1	1	0	0	1	

ID2: 0--->6 layer
1--->8 layer

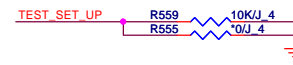
System ID: 0--->KL5
1--->KL6

CPU_ID: 0--->35W
1--->45W



SV_SET_UP

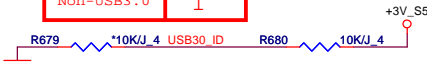
High = Strong (Default)



USB30_ID → GPIO24

USB3.0 → 0

Non-USB3.0 → 1



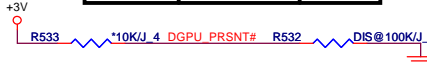
HOST_ALERT#1_R → R508 → 1K/J_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532



MFG-TEST

MFG_MODE → R184 → 10K/J_4

MFG_MODE → R194 → 10K/J_4



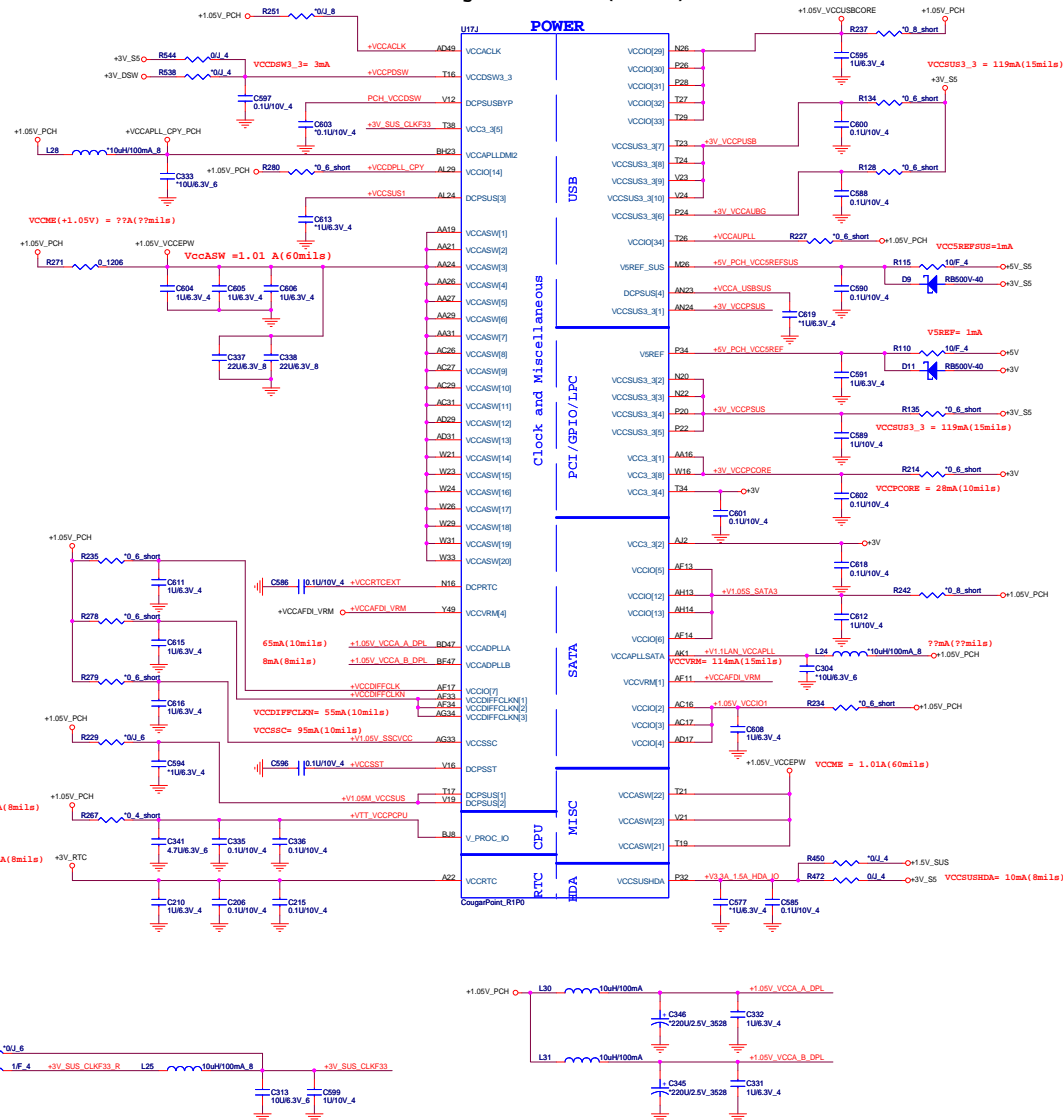
PROJECT : KL6A

Quanta Computer Inc.

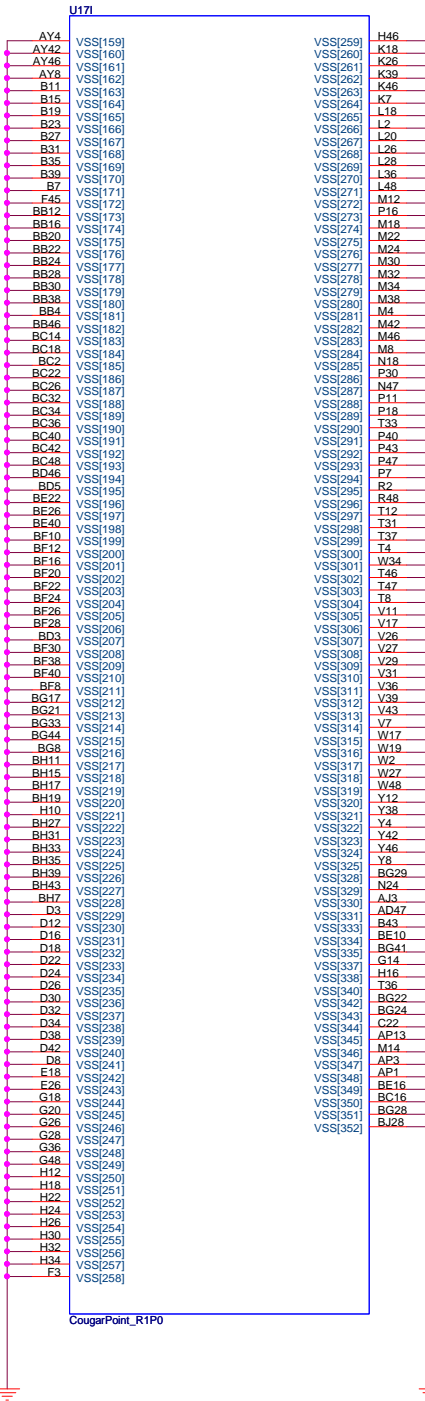
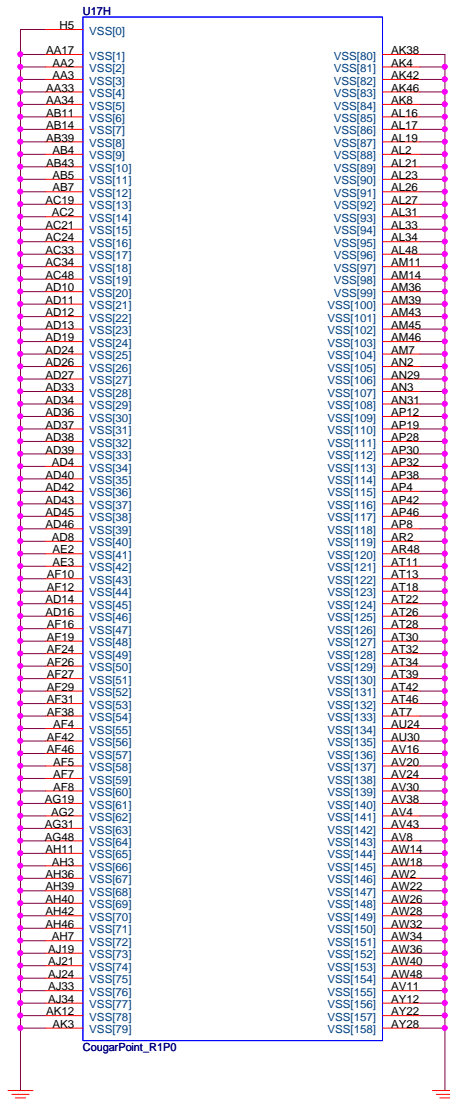
Size	Document Number	Rev
	Cougar Point 4/6	1A

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Cougar Point-M (POWER)

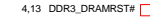
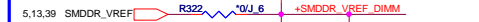
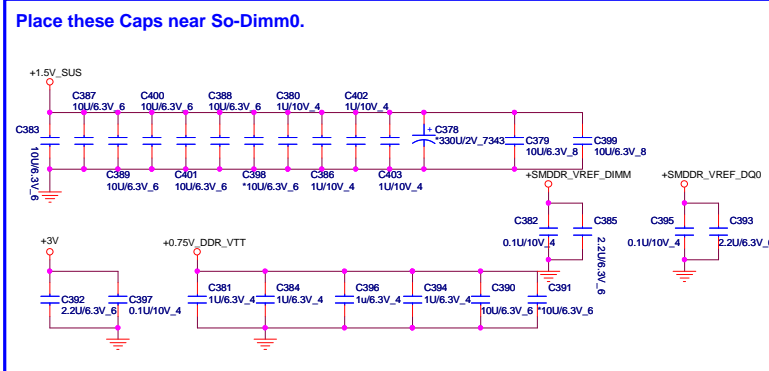


IBEX PEAK-M (GND)

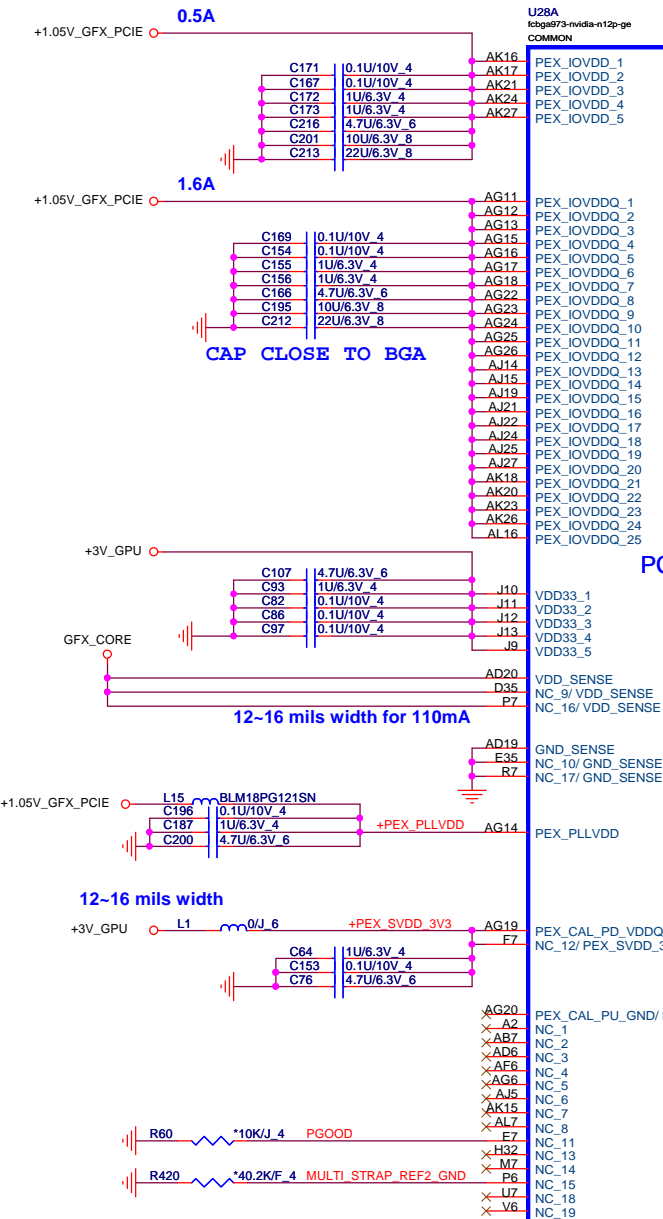




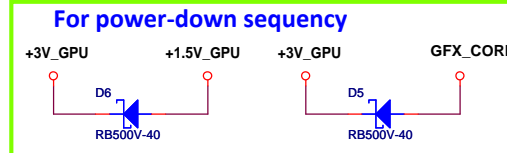
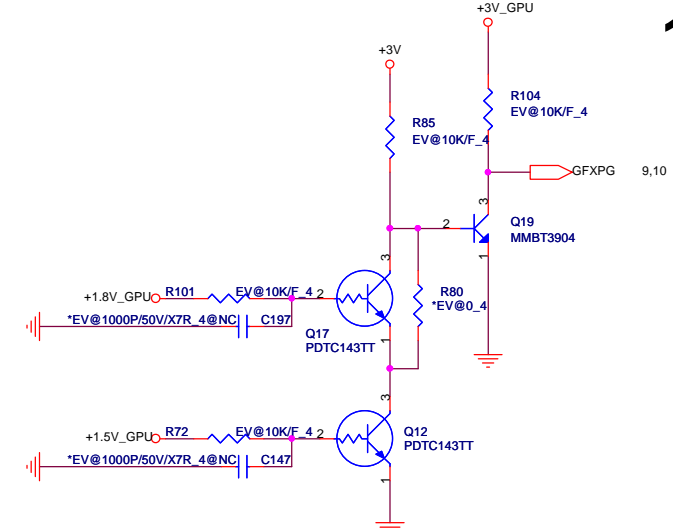
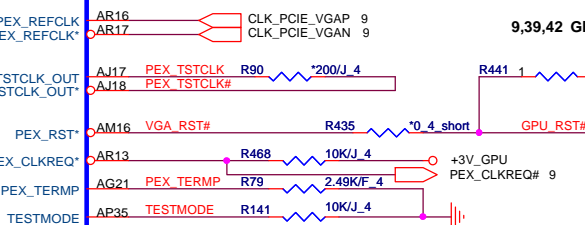
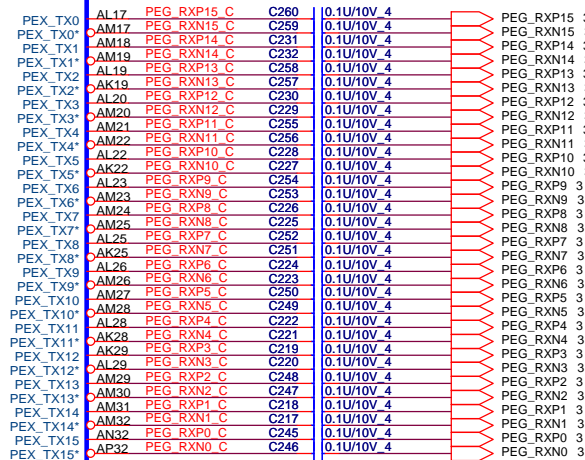
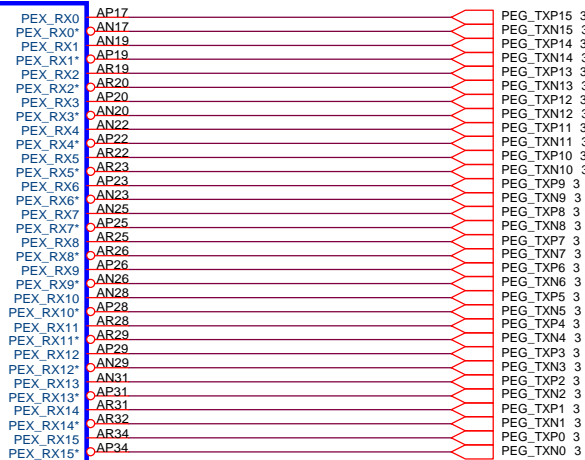
VREF DQ1 M2 Solution

Standard 4H type:DDR-C-2013289-204p

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A

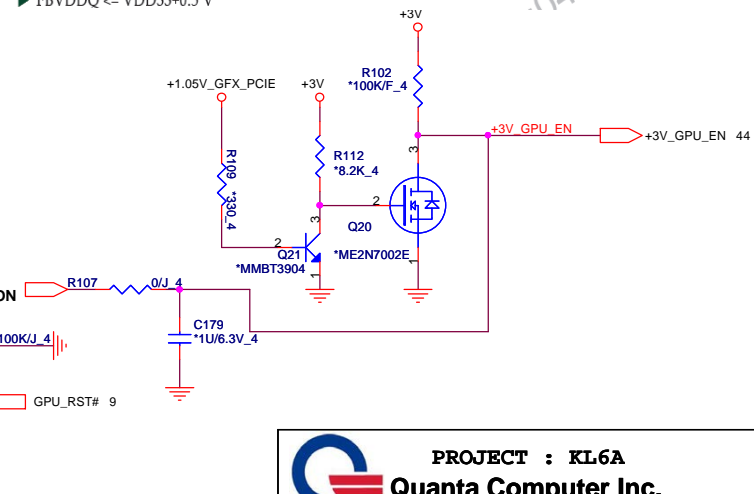


PCI EXPRESS

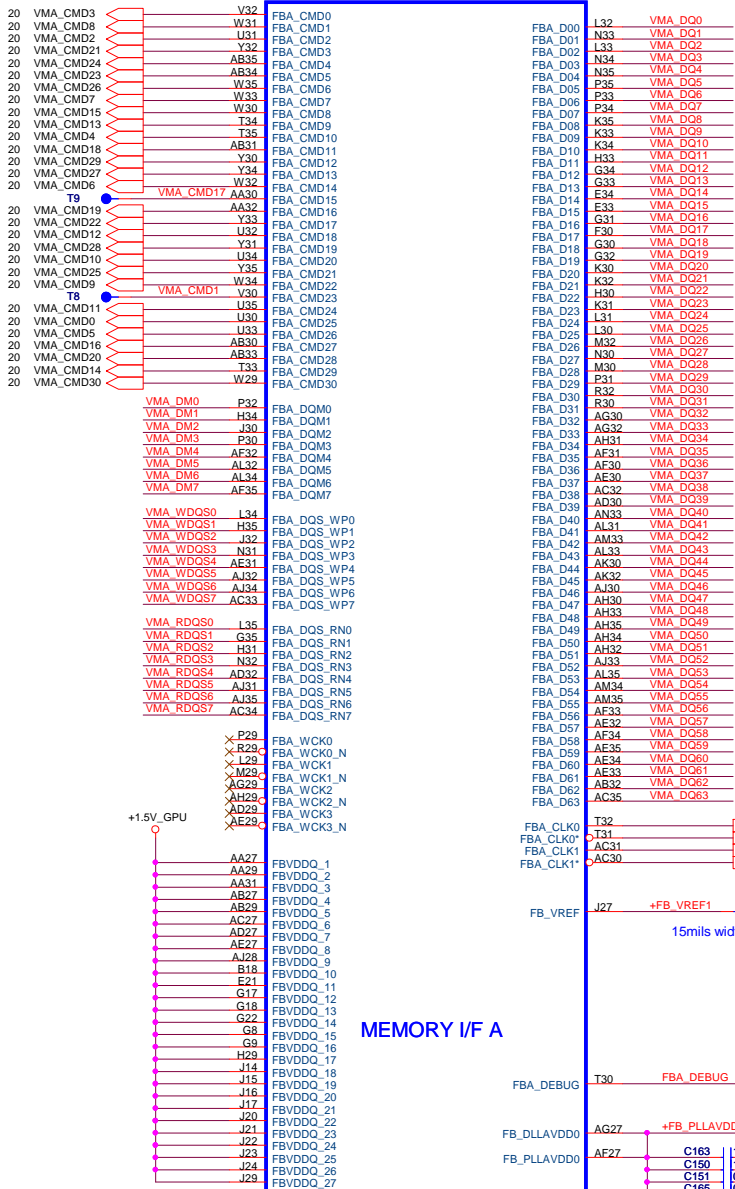


The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

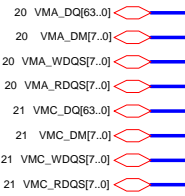
- ▶ NVDD <= VDD33+0.5 V
- ▶ FBVDDQ <= VDD33+0.5 V



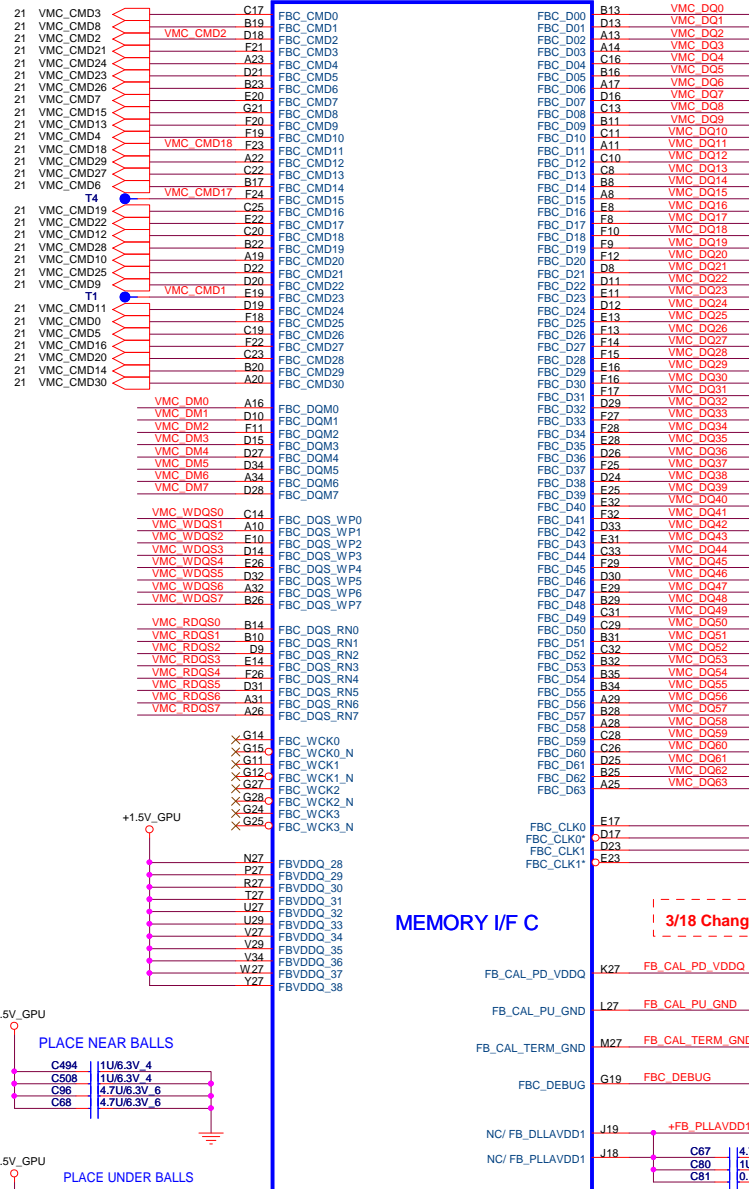
U28B

fbga973-nvda-n12p-gp
COMMON

MEMORY I/F A



U28C

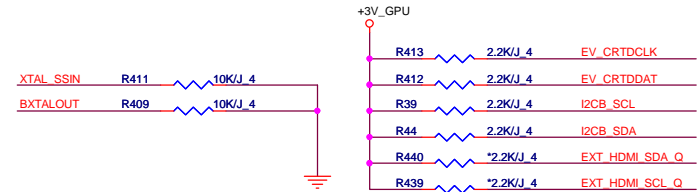
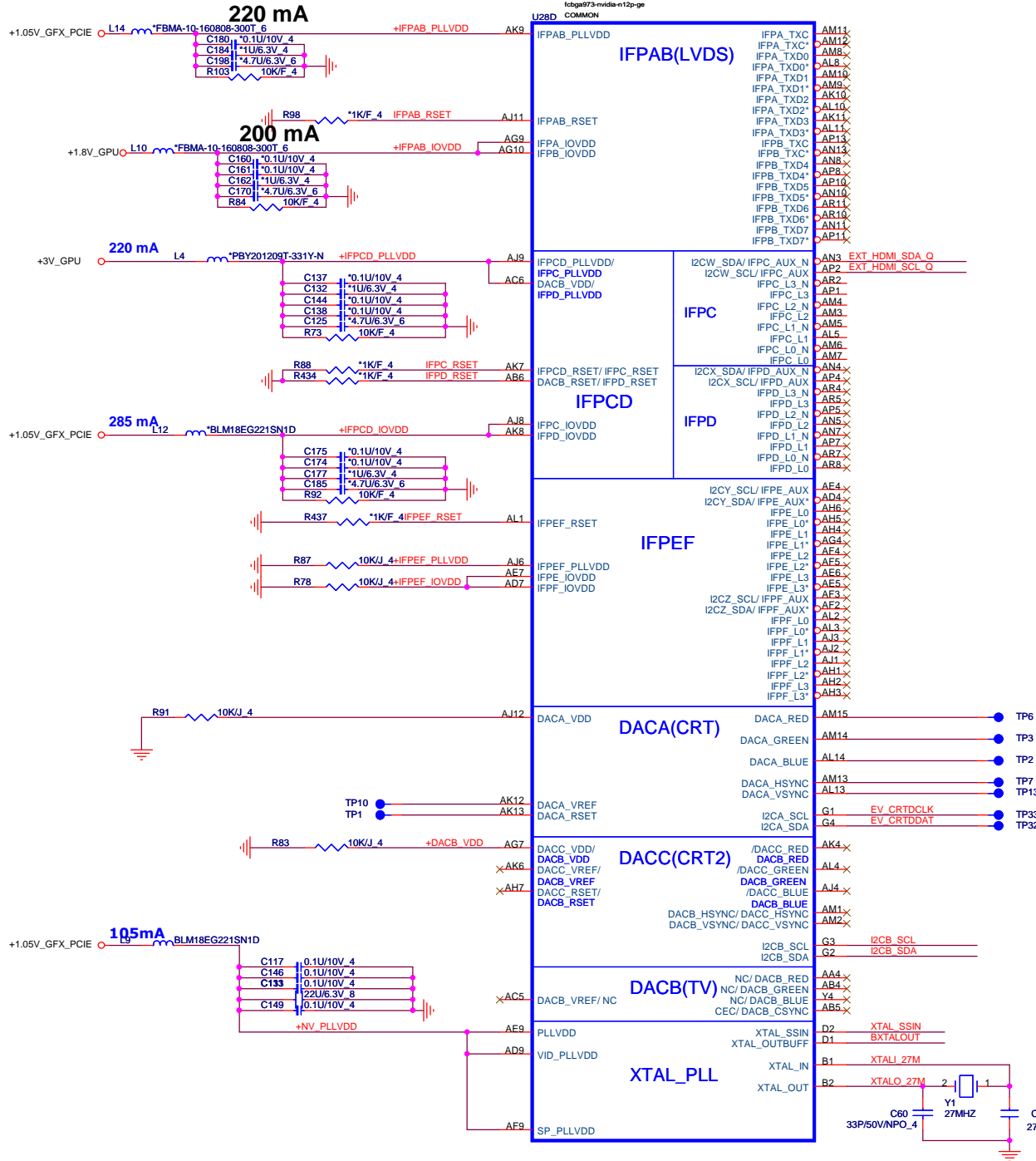
fbga973-nvda-n12p-gp
COMMON

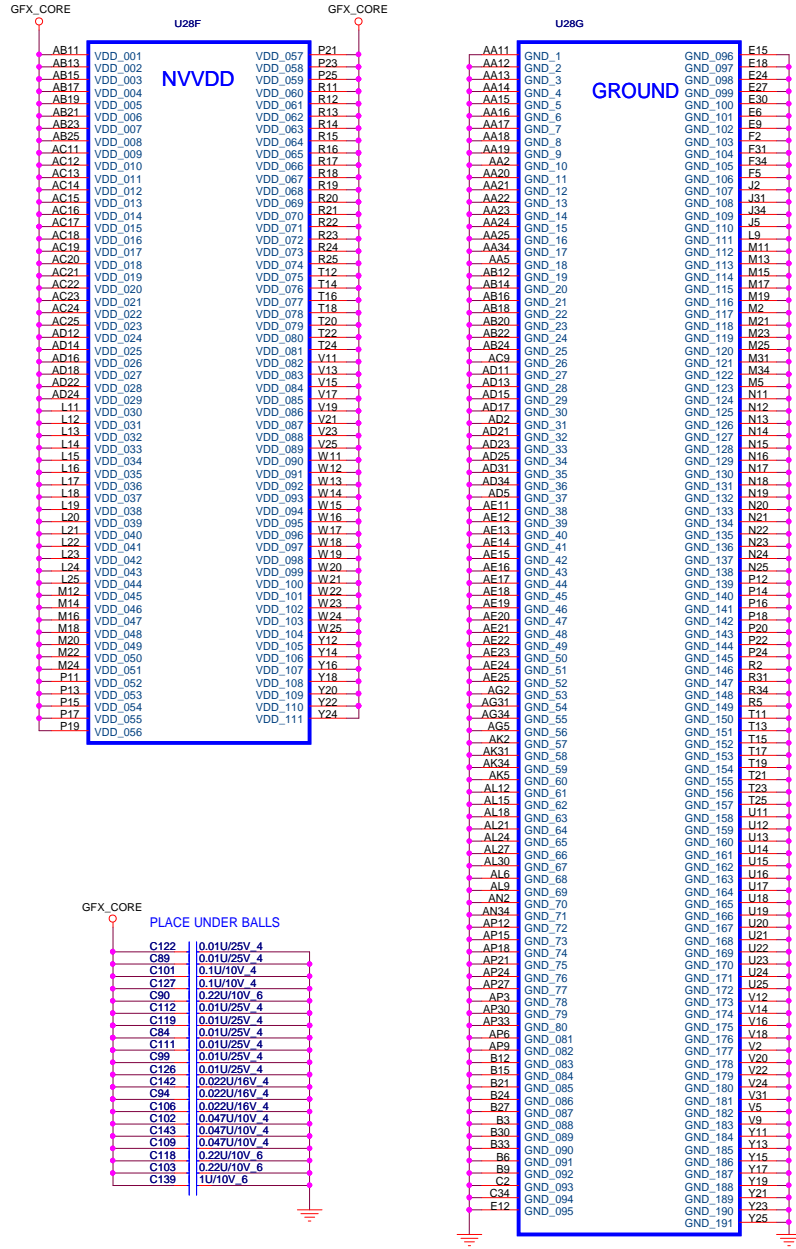
MEMORY I/F C

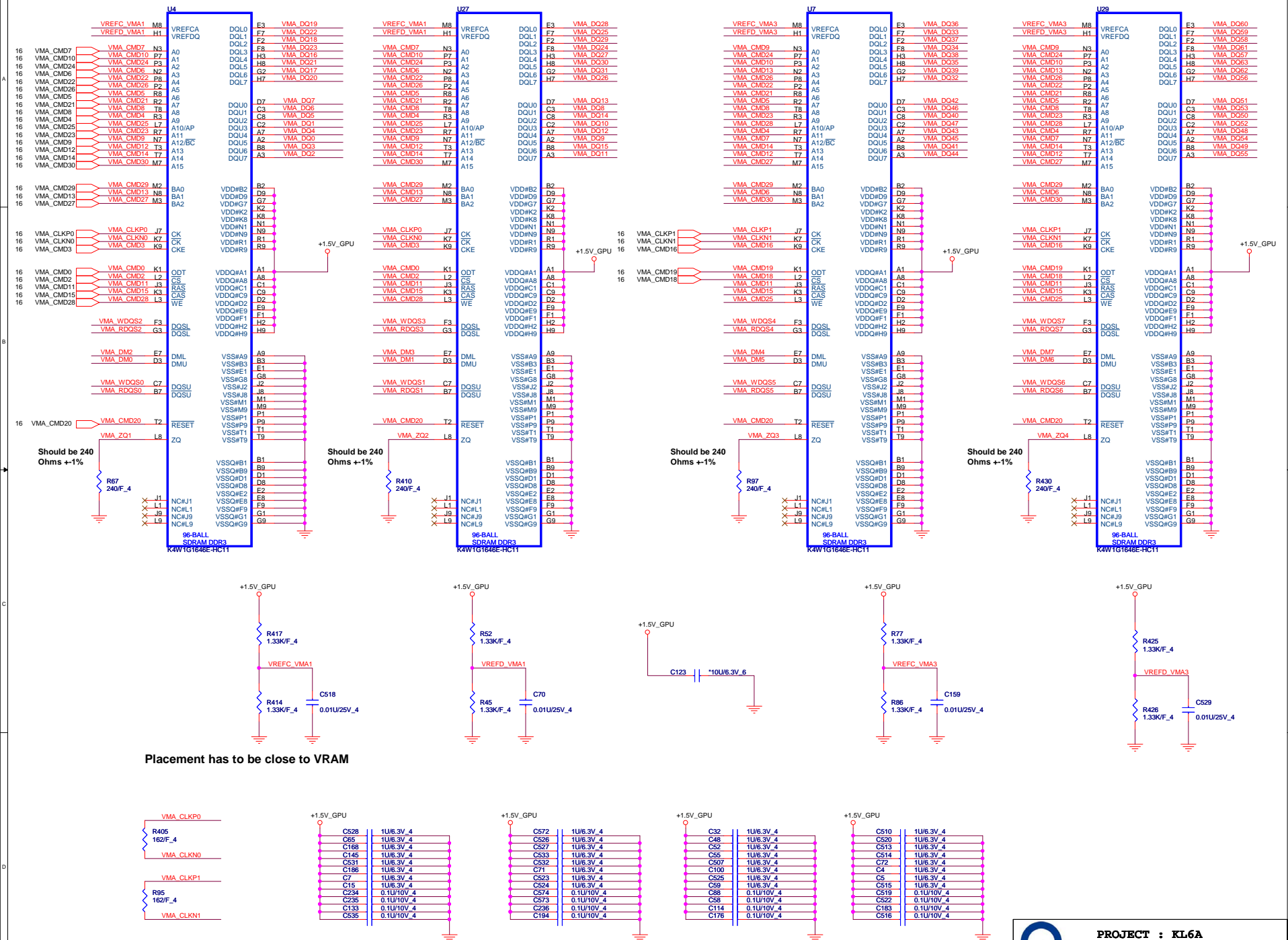
PROJECT : KL6A
Quanta Computer Inc.

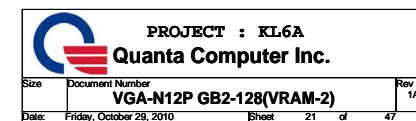
Size: Document Number: Rev 1A
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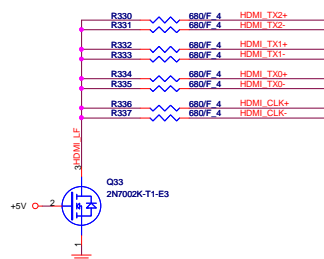
4/28 Enable LVDS For 3DV

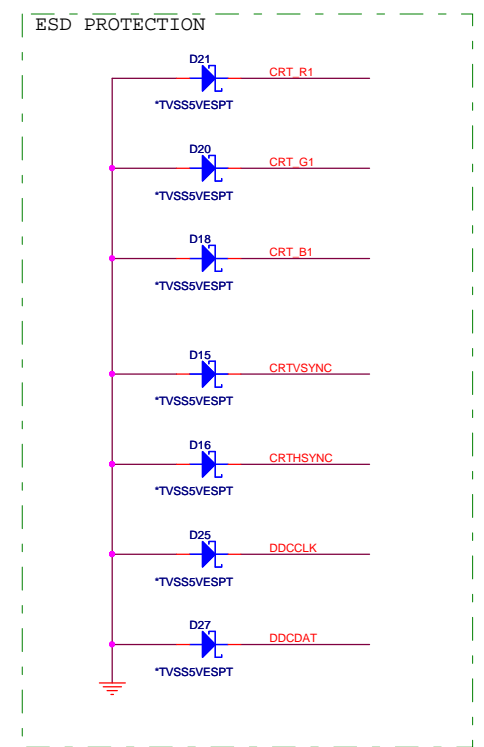
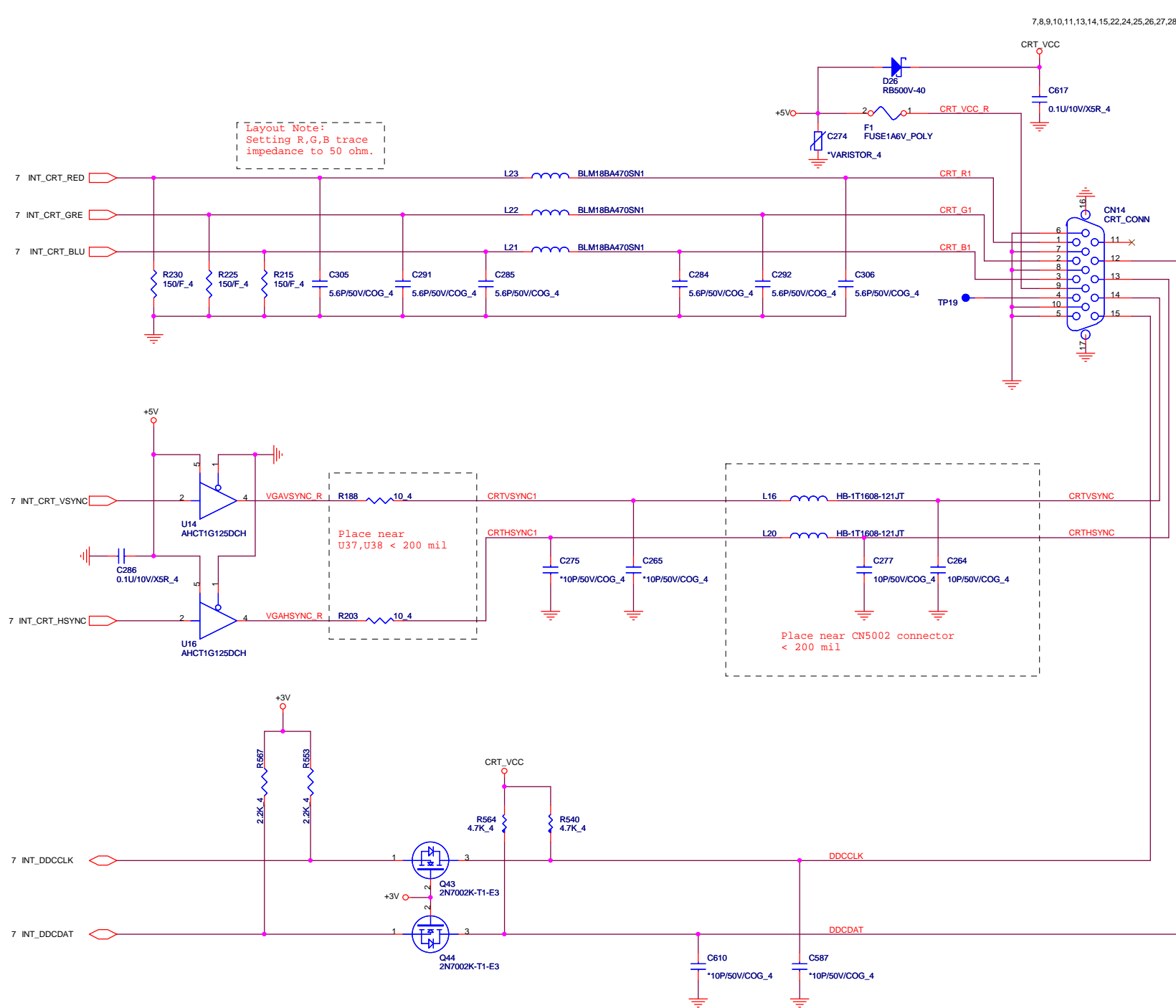




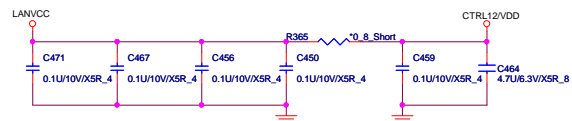
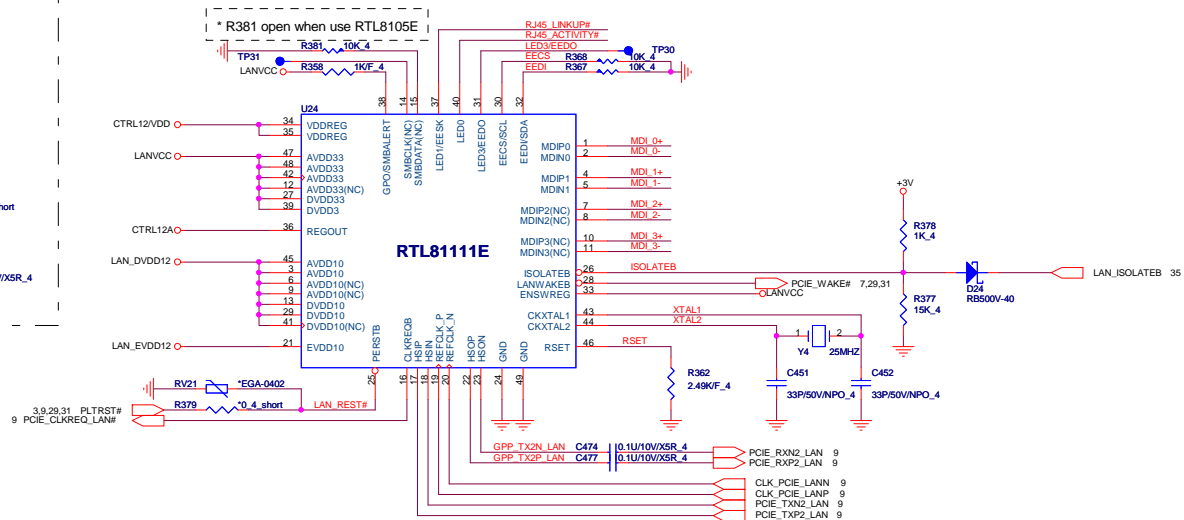
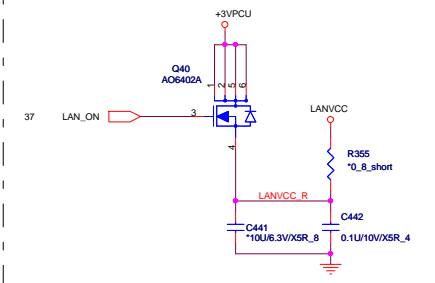






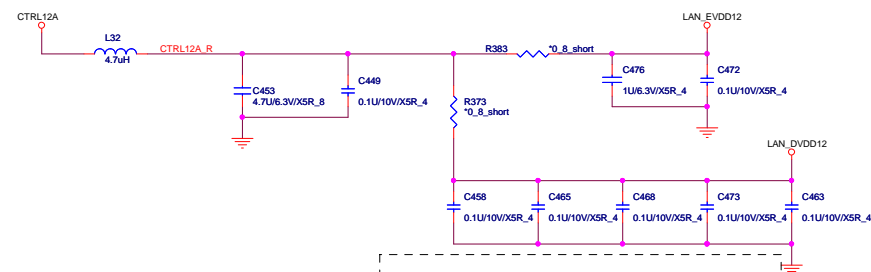


LANVCC



* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

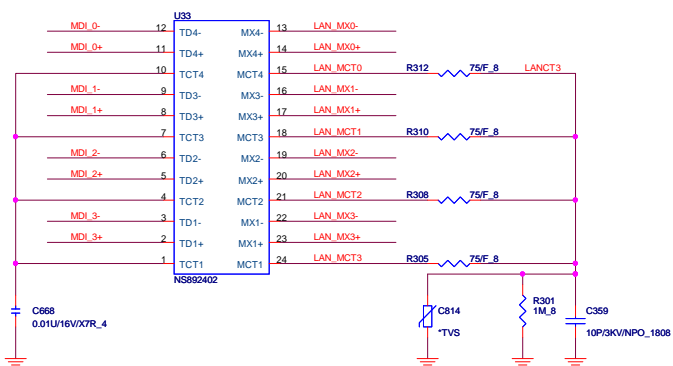
Place C5113, C5094 closed to U5006 pins 44, 45, and 40.



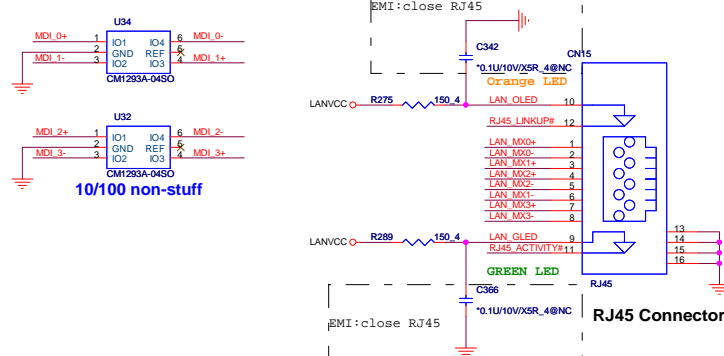
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout: All termination signal should have 20 mil trace

Transformer

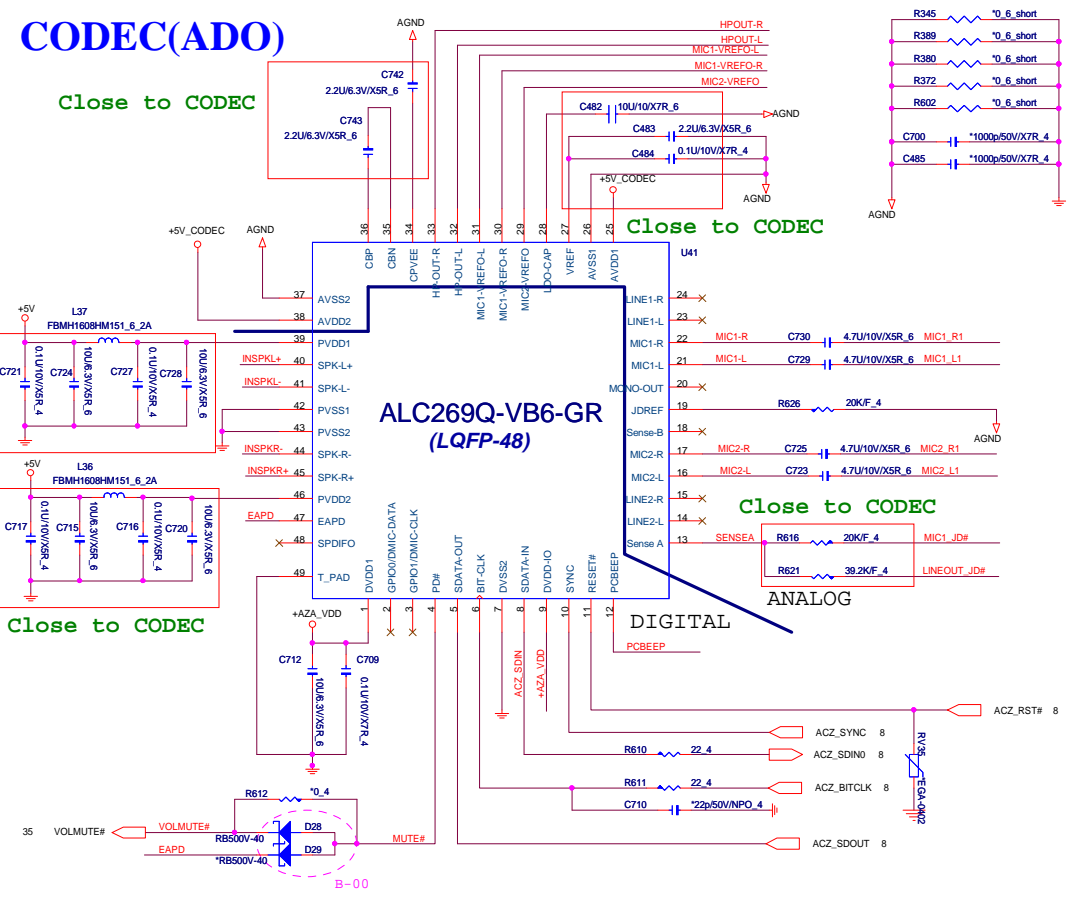


RJ45 Connector



CODEC(ADO)

Close to CODEC



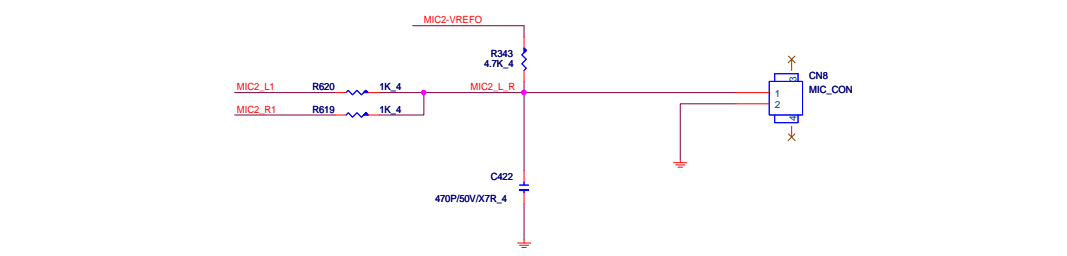
ALC269Q-VB6-GR
(LQFP-48)

Close to CODEC

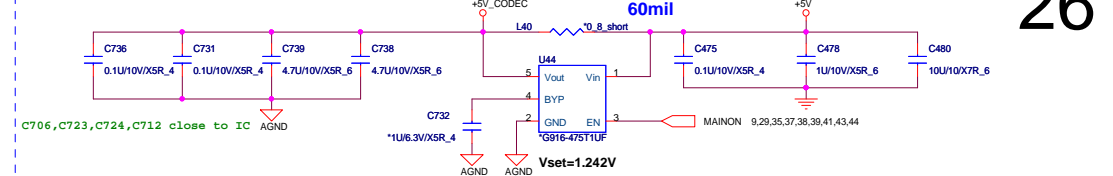
ANALOG

DIGITAL

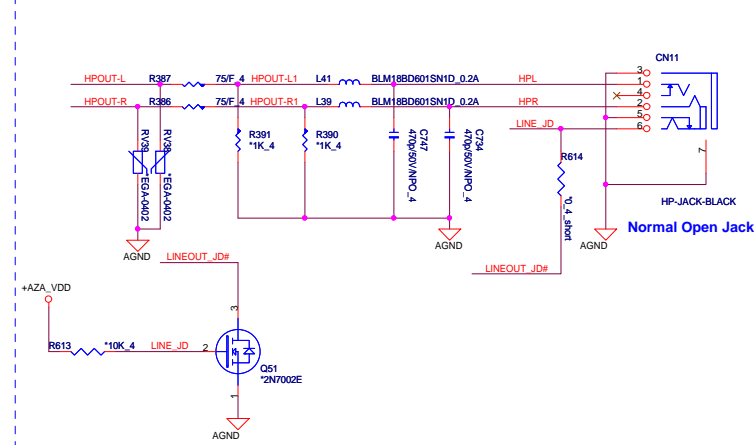
INTERNAL MIC



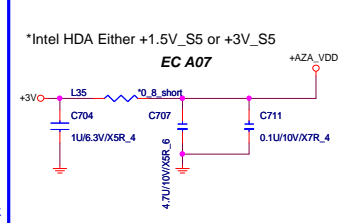
Codec Power(ADO)



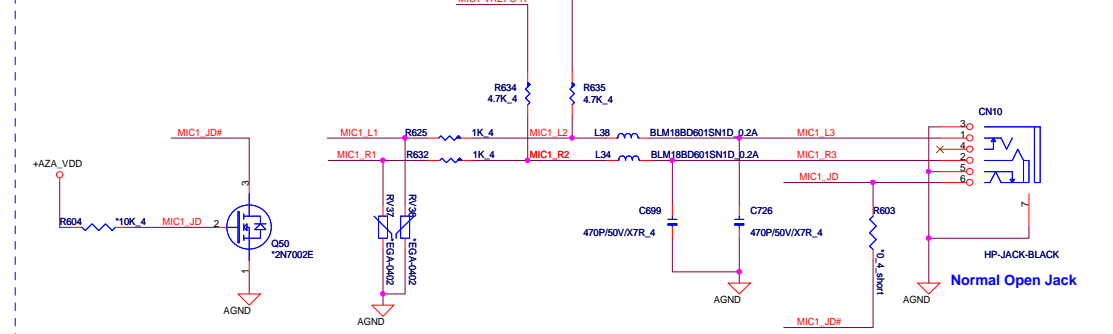
Earphone(AMP)



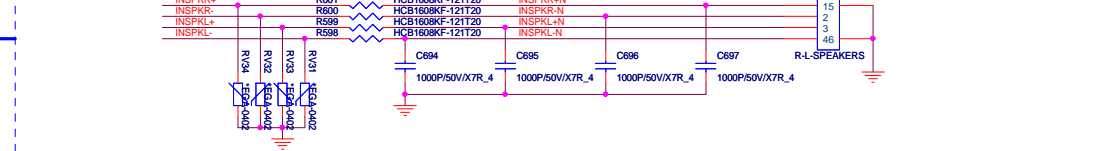
HDA Power(ADO)



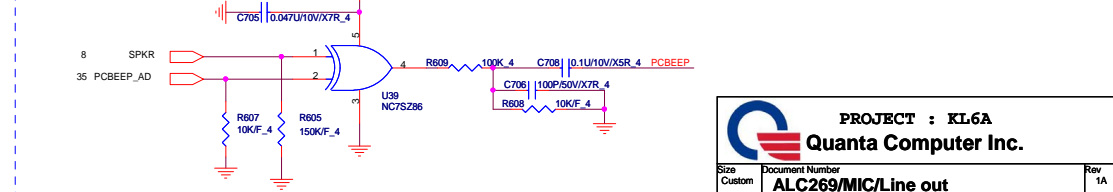
System MIC(AMP)



Speaker(AMP)



PC BEEP

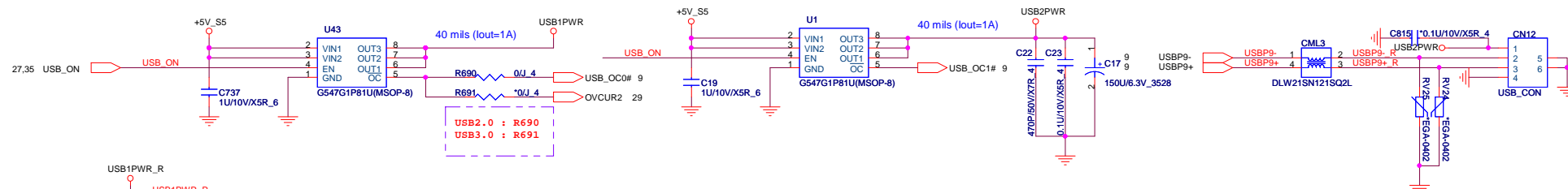


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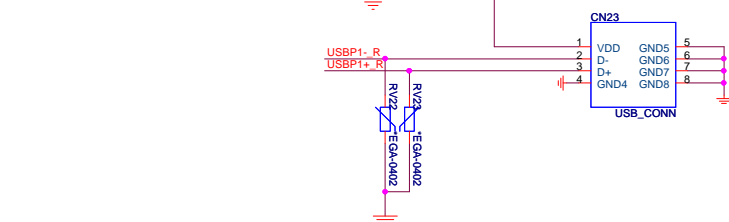
USB2.0*3

USB#1 Daughter board



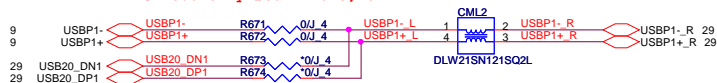
USB3.0 non-stuff CN23

USB#0 Left

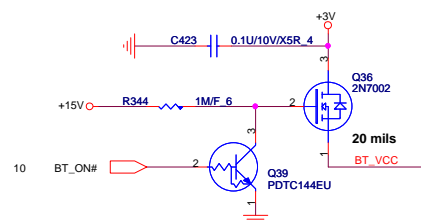
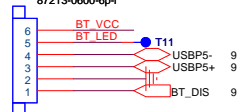


USB2.0 only stuff R671,R672

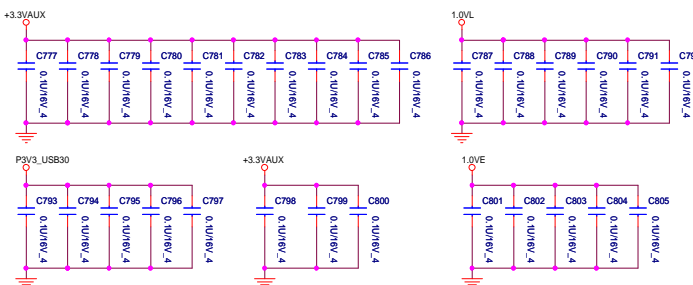
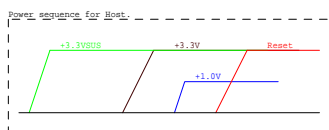
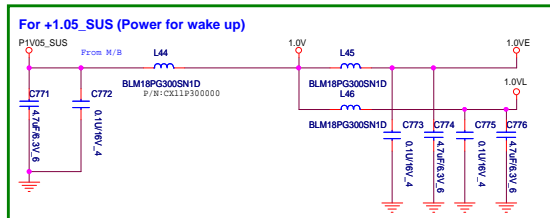
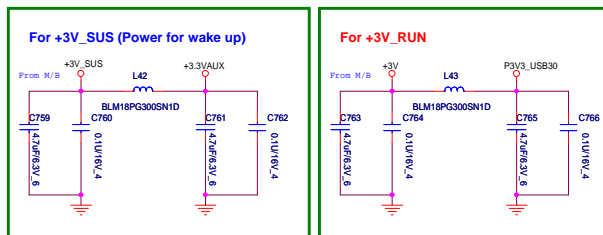
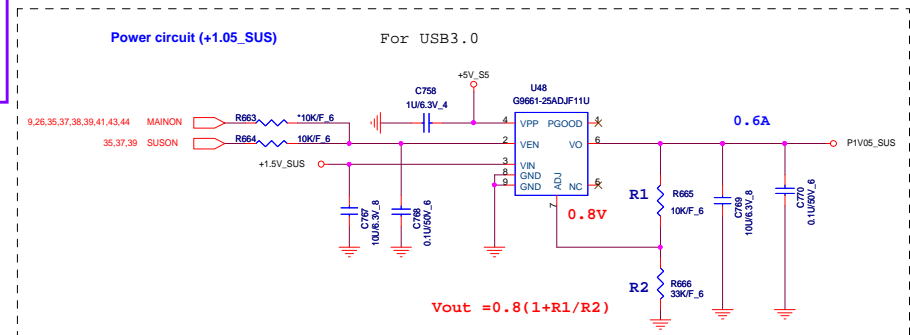
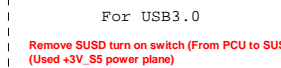
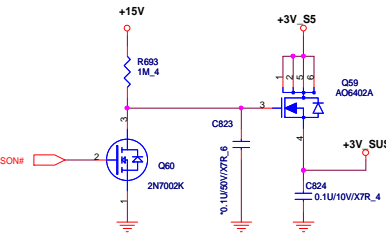
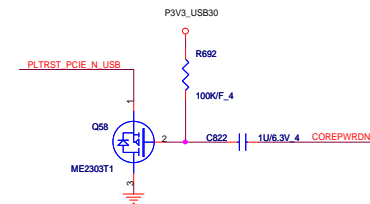
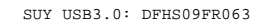
USB3.0 only stuff R673,R674



BLUETOOTH

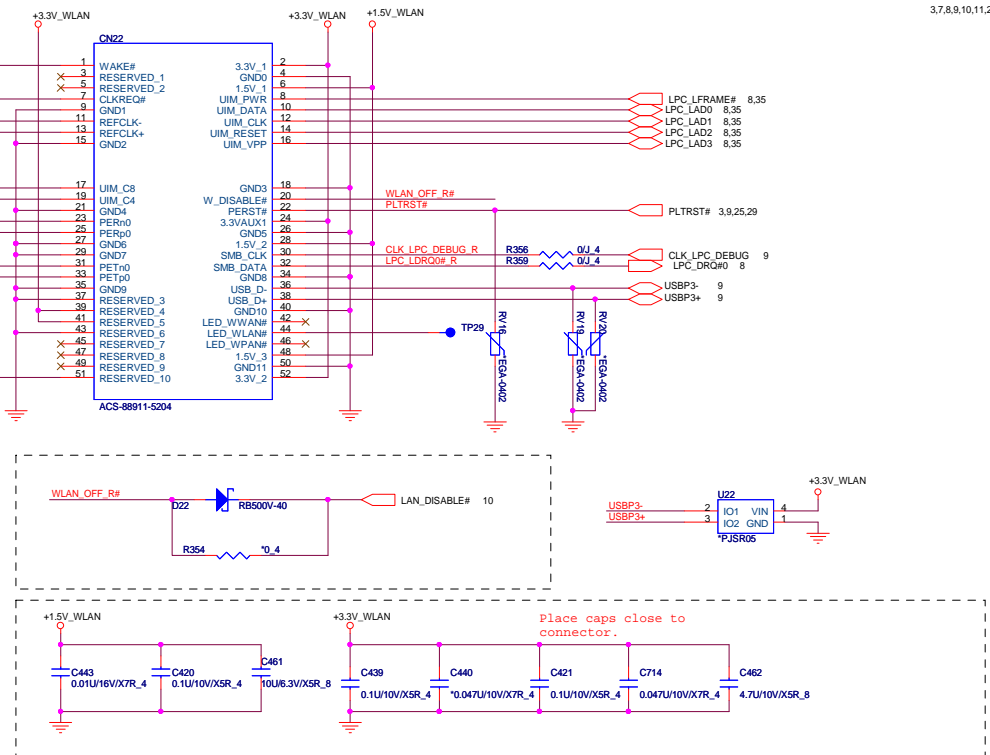
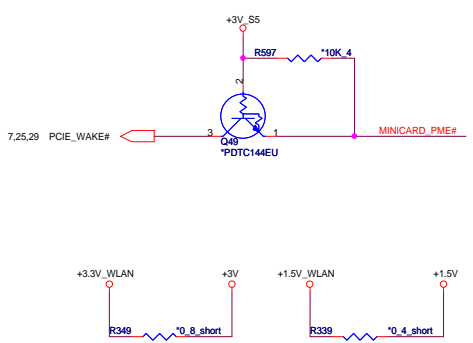
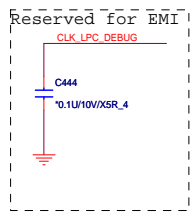
CN6
BLUE TOOTH CONN
87213-0600-6p4

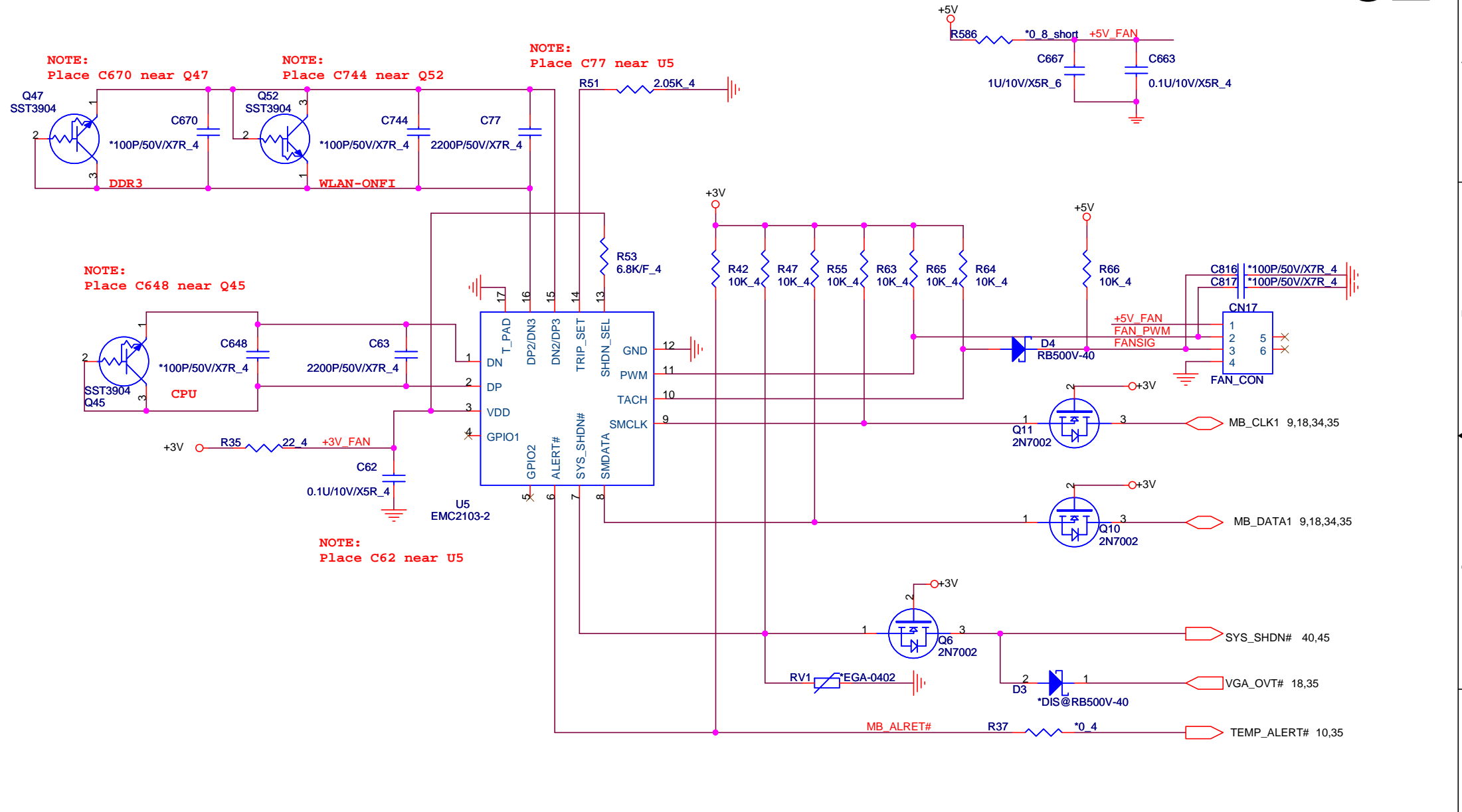
USB3.0 PORT1




WWW.AliSaler.Com

MiniCard WLAN connector





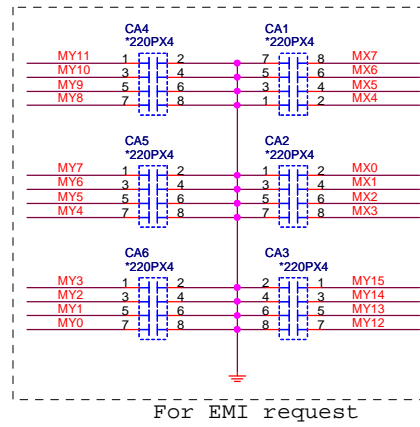
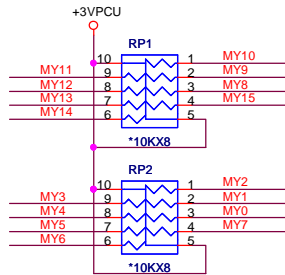
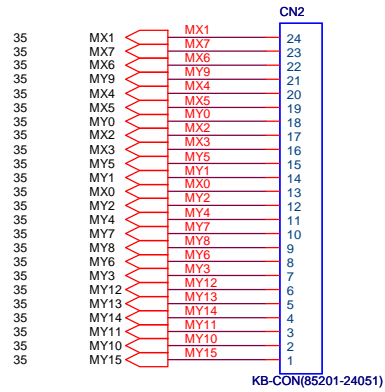


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KEYBOARD



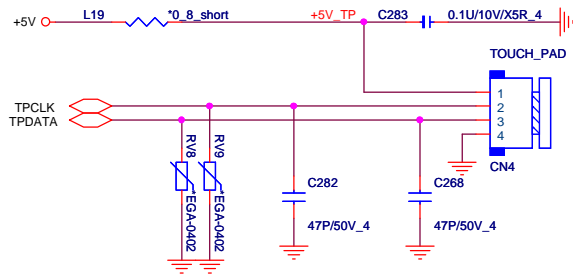
7,8,11,22,23,26,27,32,34,35,36,37,38,45
7,8,24,25,27,34,35,37,38,40,41

+5V
+3VPCU

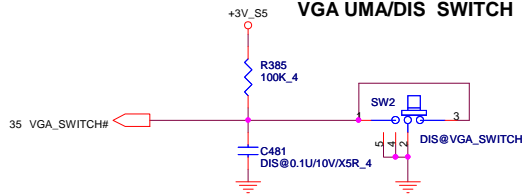


33

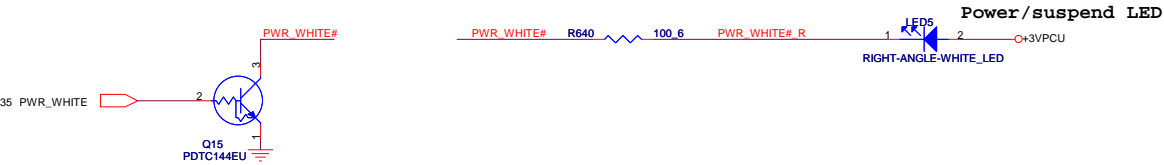
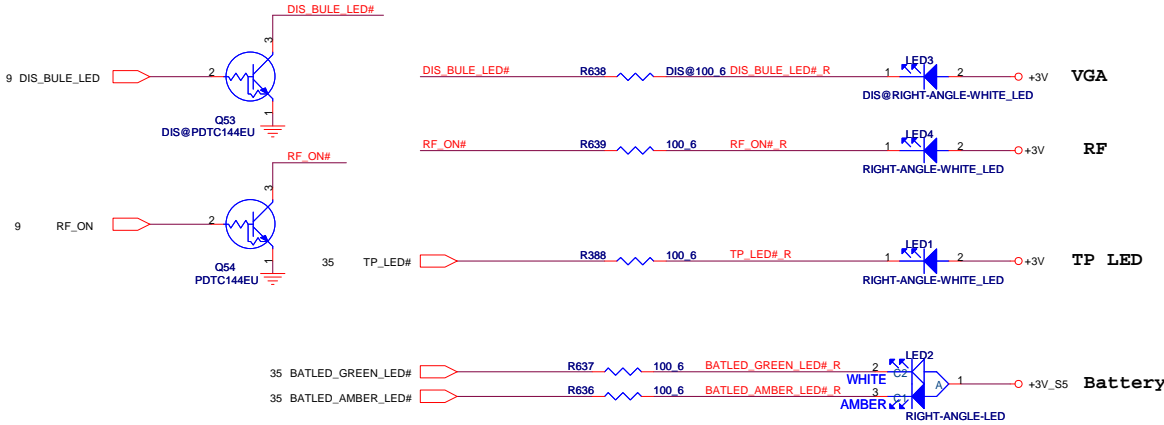
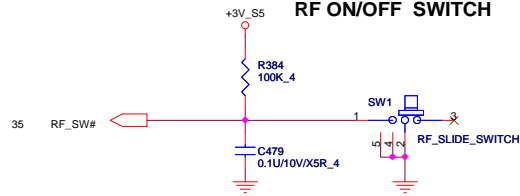
Touch pad



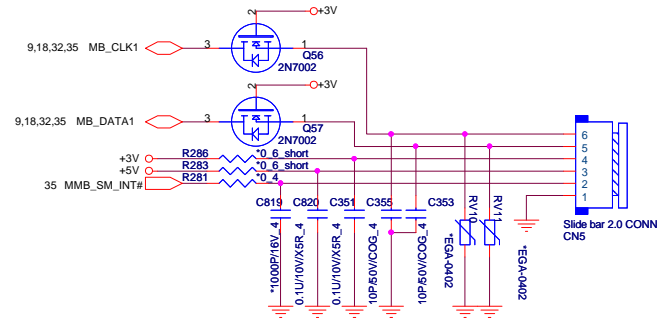
VGA UMA/DIS SWITCH



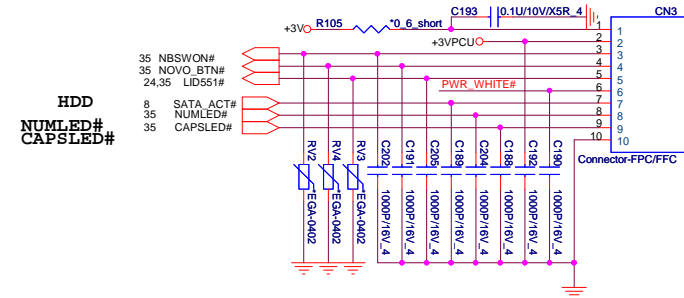
RF ON/OFF SWITCH



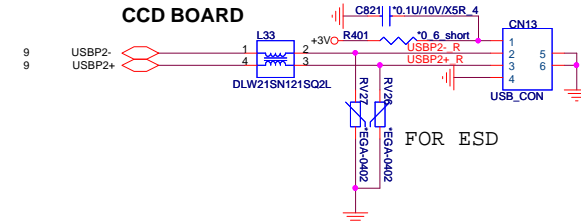
CAPACITANCE BUTTON BOARD



POWER BOARD



CCD BOARD

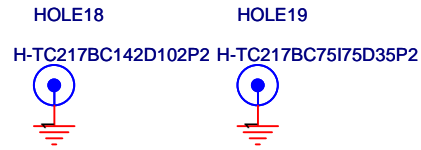


FOR ESD

Screw for ME

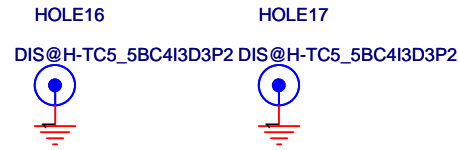
CPU BKT

WLAN

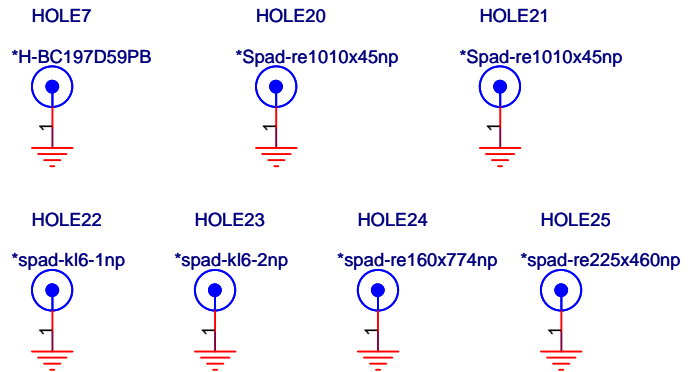
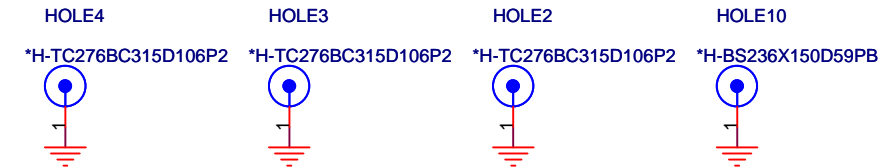
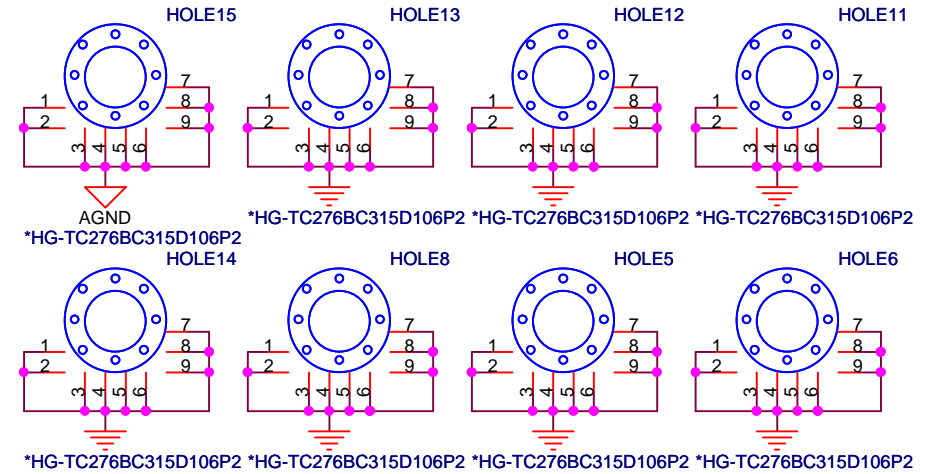
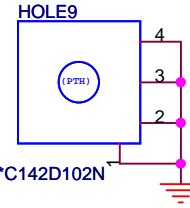


SMT NUT H=4 / 7mm

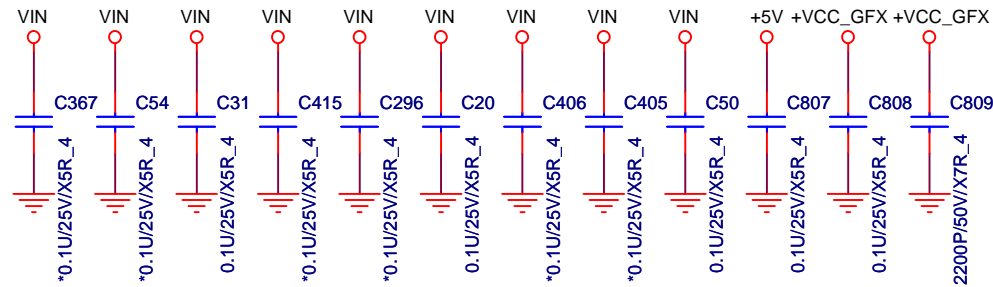
VGA



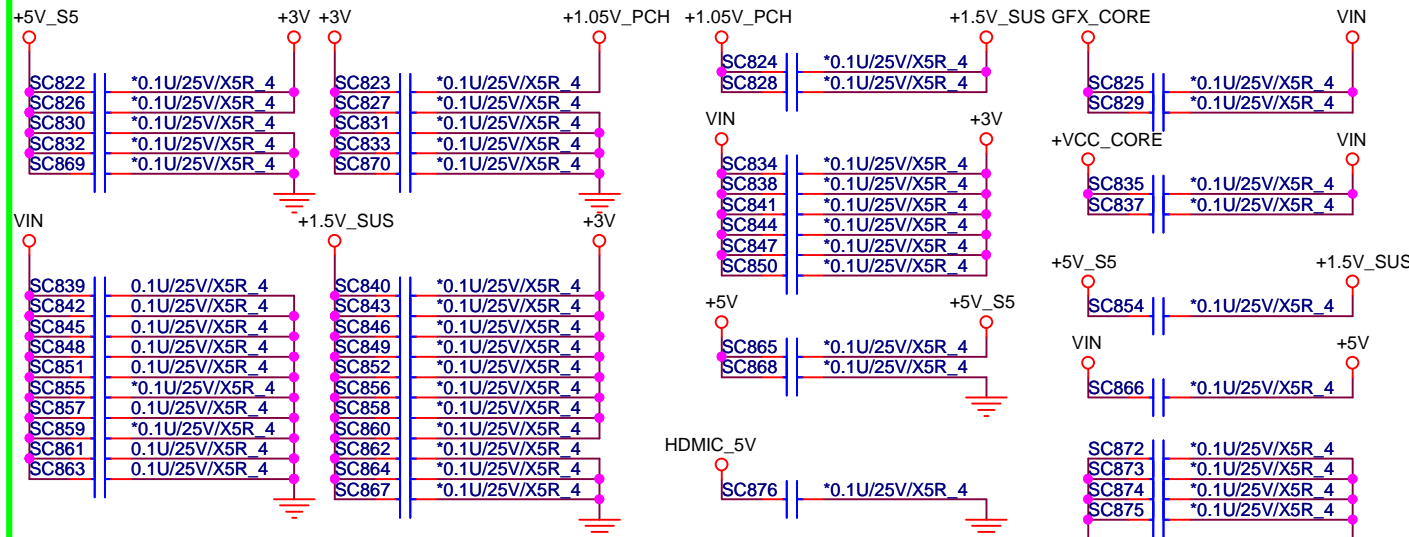
SMT NUT H=4 / 7mm



EMI suggestion



B-08

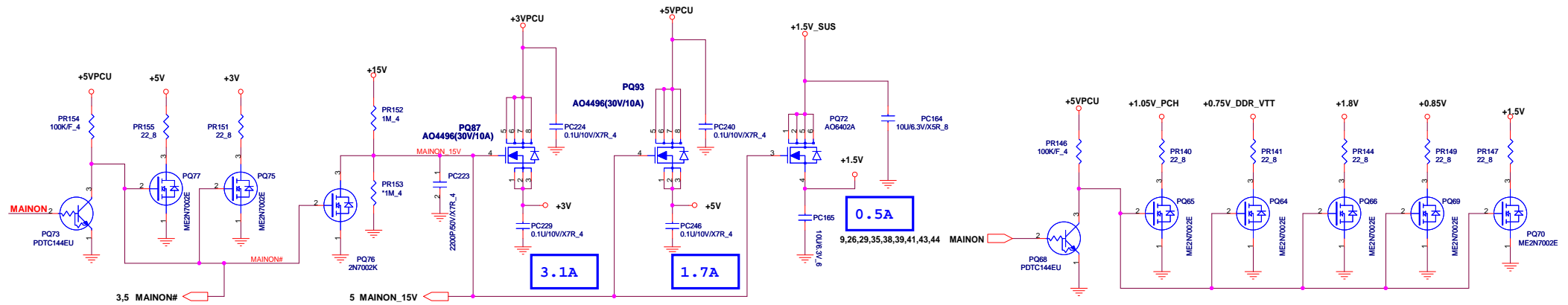


ESD suggestion

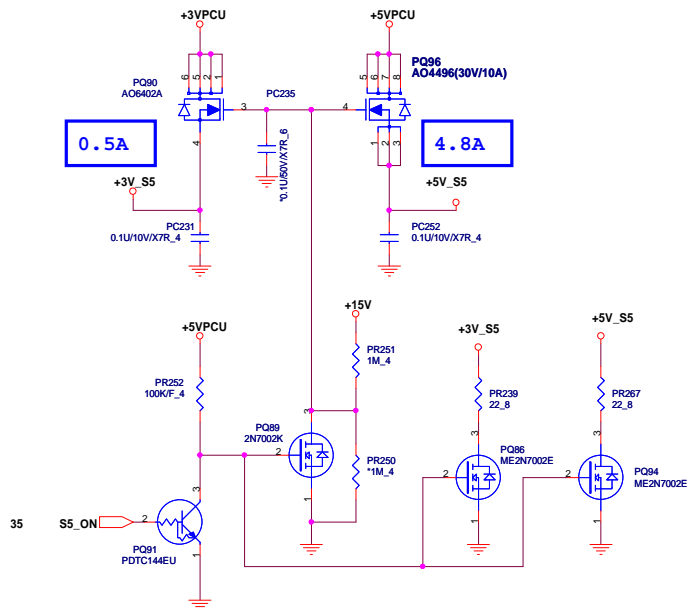
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+3V, +5V, +1.5V



3V_S5, 5V_S5



LANVCC

